Atomic Spectroscopy

Article

Analysis Of Low Power 16-Bit Processor Using Cadence - 90nm Foundry Technology

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ABSTRACT: In the era of wearable devices, there is an increasing demand for energy-efficient solutions to prolong battery life and reduce environmental impact. This work focuses on the design and implementation of low-power techniques of 16-bit processor that can be specifically tailored for IoT applications. This research presents a comprehensive exploration of the design and implementation of a 16-bit processor utilizing 90nm semiconductor technology. The design process begins with a detailed analysis of the 16-bit processor architecture, considering key components such as the Arithmetic Logic Unit, Register file, Instruction register, Mux, PC, Data Path and Controller subsystem. A systematic approach is employed to optimize critical pathways ensuring efficient data flow and reduced signal propagation delays. To leverage the benefits of 90nm technology, the design incorporates smaller feature sizes, enabling higher transistor density and improved energy efficiency. Cadence synthesis and optimization tools are employed to refine the design, considering factors such as transistor sizing, interconnect optimization, and layout considerations. The introduction of clock domain crossing mechanisms plays a pivotal role in power reduction. By dynamically controlling the 100MHz clock signals to specific modules based on their operational requirements, power consumption is significantly lowered during periods of inactivity. The design also explores trade-offs between power savings and potential impacts on performance, ensuring a balanced and efficient system. Simulation results and performance metrics are presented to validate the effectiveness of the proposed 16-bit processor design. This research contributes to the ongoing efforts in developing energy-efficient processors, providing valuable insights into the synergies between advanced semiconductor technologies and power optimization techniques. The findings are relevant for the design and implementation of processors in applications where power efficiency is a critical consideration, such as IoT based portable devices and energy-constrained environments. The power dissipation using 90nm is 1478912.42111nw for full-data path with 19052 instances & 327683.6475nw for controller with 211 cells.

Keywords: Low Power, 16-bit Processor, 90nm, Power dissipation, Dynamic-power, Static-Power, CDC.

INTRODUCTION

Design of Processor is always essential, due to its extensive usage. Of all 16-bit processors are important in embedded systems due to their versatility, cost-effectiveness, power efficiency, and suitability for a wide range of applications spanning industries such as automotive, medical, consumer electronics, and IoT. Their adoption continues to thrive as technology evolves and demands for efficient embedded solutions persist across various domains that provide the balance between performance, power efficiency, and cost. 16-bit processors are often more cost-effective compared to higher-bit processors. They provide a good balance between performance and cost, making them suitable for applications with budget constraints, such as consumer electronics and low-cost embedded systems. 16-bit processors typically consume less power compared to higher-bit processors. This makes them suitable for battery-powered devices and applications where power efficiency is critical, such as portable devices, IoT nodes, and sensor nodes. Many embedded systems require real-time processing capabilities, such as in control systems, automotive applications, and industrial automation. The simplicity and efficiency of 16-bit processors make them well-suited for real-time applications where quick decision-making and response times are essential. 16-bit processors often come with integrated peripherals and interfaces, simplifying the design of embedded systems. This integration reduces the need for additional components, leading to a more compact and cost-effective overall system. In applications where communication and connectivity are key, such as in networking devices and communication

modules, 16-bit processors provide sufficient processing power to handle data transfer and protocol handling while maintaining a reasonable level of energy efficiency. In the automotive industry, 16-bit processors are commonly used in various control units, including engine control units (ECUs), airbag systems, and anti-lock braking systems (ABS). Their real-time processing capabilities are well-suited for controlling critical functions in vehicles. 16-bit processors are employed in medical devices, including portable diagnostic tools, patient monitoring systems, and infusion pumps. The combination of processing power, low power consumption, and cost-effectiveness makes them ideal for medical applications. In consumer electronics, 16-bit processors are often found in devices such as digital cameras, handheld gaming consoles, and home appliances. Their cost-effectiveness and power efficiency contribute to the widespread use in these applications. With the growing prevalence of IoT, 16-bit processors are used in various IoT devices, including smart sensors, wearable's, and home automation systems. Their ability to perform basic tasks efficiently aligns well with the requirements of many IoT applications. The Design Metrics collectively provide a comprehensive view of a processor's performance, balancing speed, power efficiency, and resource utilization. Designers often optimize these metrics based on the specific requirements of the target application and the constraints of the embedded system. key metrics used to evaluate the performance of a processor are stated below Clock Frequency, the clock frequency, measured in Hertz (Hz) or megahertz (MHz), represents the rate at which the processor's internal operations are synchronized. Higher clock frequencies generally indicate faster processing capabilities. However, it's crucial to consider power consumption and heat dissipation, as increasing clock frequency may lead to higher power requirements. Throughput, the throughput measures the amount of data processed per unit of time and is often expressed in bits per second (bps) or transactions per second (TPS). Throughput provides a broader perspective on the processor's overall performance, considering both the clock frequency and the efficiency of instruction execution. IPC represents the average number of instructions executed per clock cycle. A higher IPC value indicates better efficiency in executing instructions, which can contribute to improved performance without solely relying on increased clock frequencies. Power consumption measures the amount of electrical power consumed by the processor during operation and is often expressed in watts (W). Low power consumption is critical for battery-powered devices and applications where energy efficiency is a priority. Power efficiency is evaluated across different operational states, including active, idle, and sleep modes. Energy efficiency is a measure of how effectively the processor performs computations while minimizing power consumption. It combines performance and power consumption metrics to assess how much energy is used to complete a specific task. Energy efficiency is crucial for portable and battery-operated devices. Area utilization measures the physical size of the processor on the chip and is often expressed in square millimeters. Efficient use of silicon real estate is important for cost-effective designs. Smaller processors with optimized layouts can contribute to reduced manufacturing costs and increased integration possibilities. CPI measures the average number of clock cycles required to execute one instruction. A lower CPI indicates better efficiency in instruction execution. CPI is closely related to IPC and helps assess how well the processor utilizes each clock cycle. Cache performance metrics include hit rate, miss rate, and latency in accessing the cache memory. Cache efficiency impacts overall processor performance. Higher hit rates and lower miss rates contribute to improved performance by reducing memory access latency. Latency measures the time delay between initiating a process and receiving the result, while response time is the total time taken to complete a task. Low latency and response times are critical in real-time applications, ensuring quick decision-making and responsiveness. FLOPS measures the number of floating-point operations a processor can perform in one second. FLOPS are crucial for applications requiring extensive floating-point calculations, such as scientific simulations and graphics processing. Clock Domain Crossing (CDC) is a crucial aspect in the design and verification of digital integrated circuits, especially in Very Large Scale Integration (VLSI) designs. In VLSI, a digital system often consists of multiple clock domains, each driven by its own clock signal. Clock domains are distinct regions of a design where the timing is controlled by a specific clock signal. Clock Domain Crossing occurs when signals or data cross between different clock domains. Managing this crossing is challenging because the clocks in different domains may have different frequencies, phases, or even be asynchronous. If not handled properly, CDC issues can lead to data synchronization problems, metastability, and ultimately impact the reliability and functionality of the digital system. When a signal crosses from one clock domain to another and violates the setup or hold time requirements, it can enter a metastable state. Metastability is an unpredictable state that can lead to incorrect data values and potentially cause the failure of the digital system. To mitigate the effects of metastability, synchronization elements such as flip-flops or double-flop synchronizers are often employed. These elements help in ensuring that data transitions between clock domains are captured reliably. Static timing analysis and formal verification are used to analyze and address CDC issues during the design and verification phases. The overall flow the work is mentioned as stated below.

Second section literature survey is conferred, third section exhibits about the proposed design, fourth section infers about obtained simulated results followed by conclusion and future scope.

LITERATURE SURVEY:

Most of the authors have emphasized on the clock gating scheme and the design of 16-bit processors, here are few representations about them. In [1] year 2017, T.C. Taranth et.al signified about the RTL synthesis using Cadence DC. In [2] year 2021, M. W. El-Kharashi et.al focused on Open Lane and Commercial Approaches in Comparison with RISC processor. In [3] 2018, Technology mediated tutorial on RISCV CPU core implementation and sign-off using revolutionary EDA management system. In [4] 2014, N Saraswati et.al, has presented Cadence based Implementation of a 32-bit MIPS. In [5] 2012, Sangmin Kim et.al, have shown the synthesis of pulsed circuits using clock gating. In [6], the authors have analysed the 16-bit ALU with clock gating technique. In [7], the authors have simulated the 16bit processor using clock-gating technique with cadence 45nm technology. In [8], the authors presented the simulation of 16-bit processor using cadence 90nm technology. In [9], Sudha et.al, have contributed the work on physical synthesis of 16-bit processor. In [10] Chandran Venkatesan et.al, have proposed the design of RISC processor using Harvard architecture. In [11] Dr. Sujatha have

implemented the design of 32 bit RISC processor. In [12], the authors have simulated the work on 32bit non-pipelined processor using cadence

Proposed Design:

This section deals with the proposed ASM design methodology & block representation. The CPU architecture method can be divided into two parts, the controller and the data path. By separating these two parts, the architecture of the device is streamlined. This application-driven design specifies the Finite State Machine (FSM) that governs the data path by the instructions to be executed. As a result, the control unit may be configured as an FSM that drives the pipeline phases that transmit signals to the data path unit to execute the operation encoded in the instruction set.

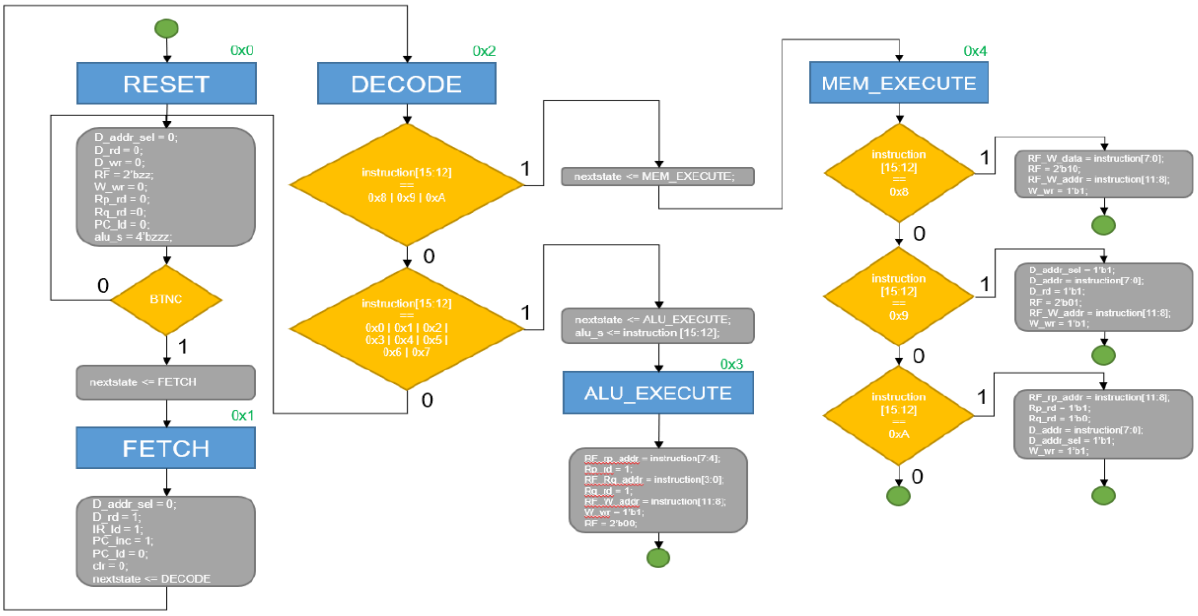

Fig A: Algorithmic State Machine.

The ASM Control Unit Map is presented in this section and was selected to present the architecture before the actions of the processor. Figure A indicates the ASM Chart Control Unit. There are 5 states in which the Control Unit cycles: Reset, Fetch, Decode, ALU Execute, and MEM Execute. The Reset state sets the control signals for both the Memory Unit and the Datapath Unit to 0. In this mode, the next state to prevent the program from cycling through all instructions without warning from the user. Next, the Retrieval State is present to recover the address from the Memory Unit and load it into the Instruction Register. After obtaining the address, the Control Unit will go to the Decode state where the Instruction will be evaluated for its opcode. Based on the opcode, the Control Unit assigns the next state either to the MEM Execute or to the ALU Execute states, the former to the load-store instructions, and the latter to the logical or arithmetic instructions. If the Control Unit runs between these two states, it returns to the Reset state and waits for the user to retrieve the next instruction.

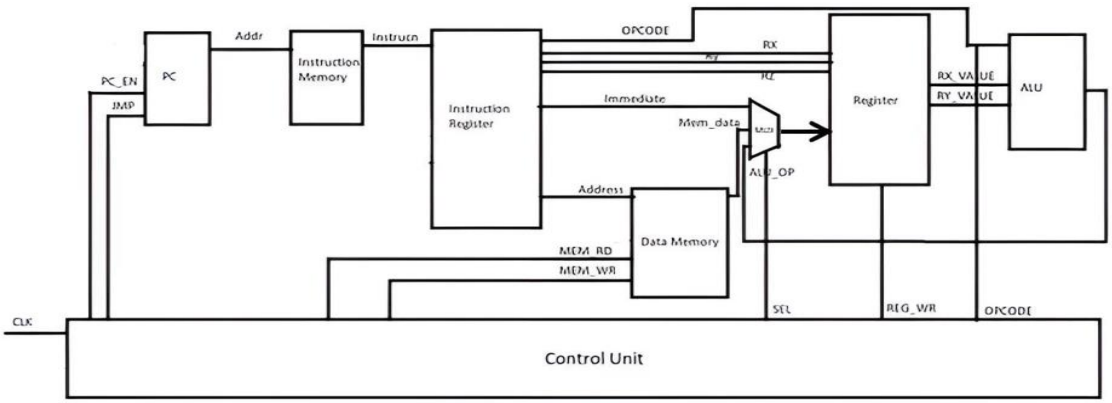

Fig B – Existing System Design[9]

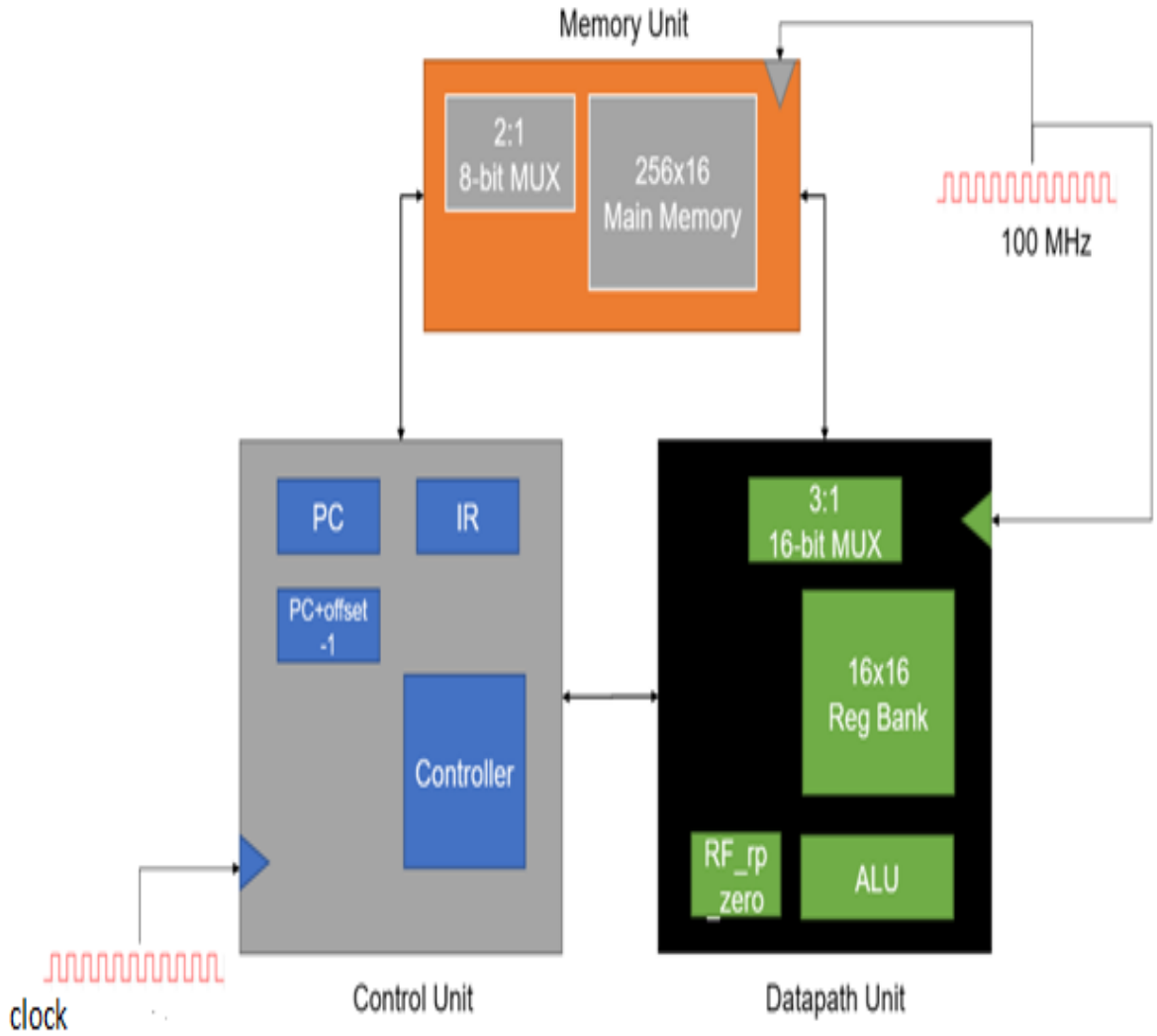

Fig C – Proposed Design of Control Unit, Memory Unit, Data path Unit

To simplify the architecture, the processor is divided into three different units: power, memory, and data path units. At a high stage, the control unit retrieves the instruction, decodes it, and sends the necessary signals to all memory and data path systems to execute the instruction. The data path unit controls access to the registry bank, performs arithmetic and logical operations, and communicates with all control and memory units. The memory unit manages access to the main memory and interacts with both control and data path drives. This high-level description is shown in Figure B and the HDL code represents this hierarchy as shown—the blocks within the units are sub modules to the unit module.

SIMULATION RESULTS:

As far as the difficulty of the configuration and execution of the Power, Datapath and Memory Units is concerned, the Control Unit was definitely the most difficult; the Memory Unit was the easiest and the Datapath Unit followed suit. First, all of the submodules, except the Controller, were designed and evaluated individually. After that, the design phase for the Memory and Datapath Systems was as follows: create and evaluate individual submodules within the Device, test the submodules in tandem, and eventually construct and test the submodule wrapper as a Device. Once the Datapath and Memory Modules were designed and tested separately, they were integrated and tested in unison. After testing the proper operation of both devices, the controller was modelled with the ASM chart displayed. Next, the HDL Controller was developed and simulated by linking the other two submodules in the Control Unit: the PC and the IR.

The next move with the Control Unit in service was to test it with the Memory Unit. The testing of the proper operation with the Datapath Unit was carried out following the Memory Unit evaluation. The Processor was eventually designed as the top module containing the Power, Memory, and Datapath Modules.

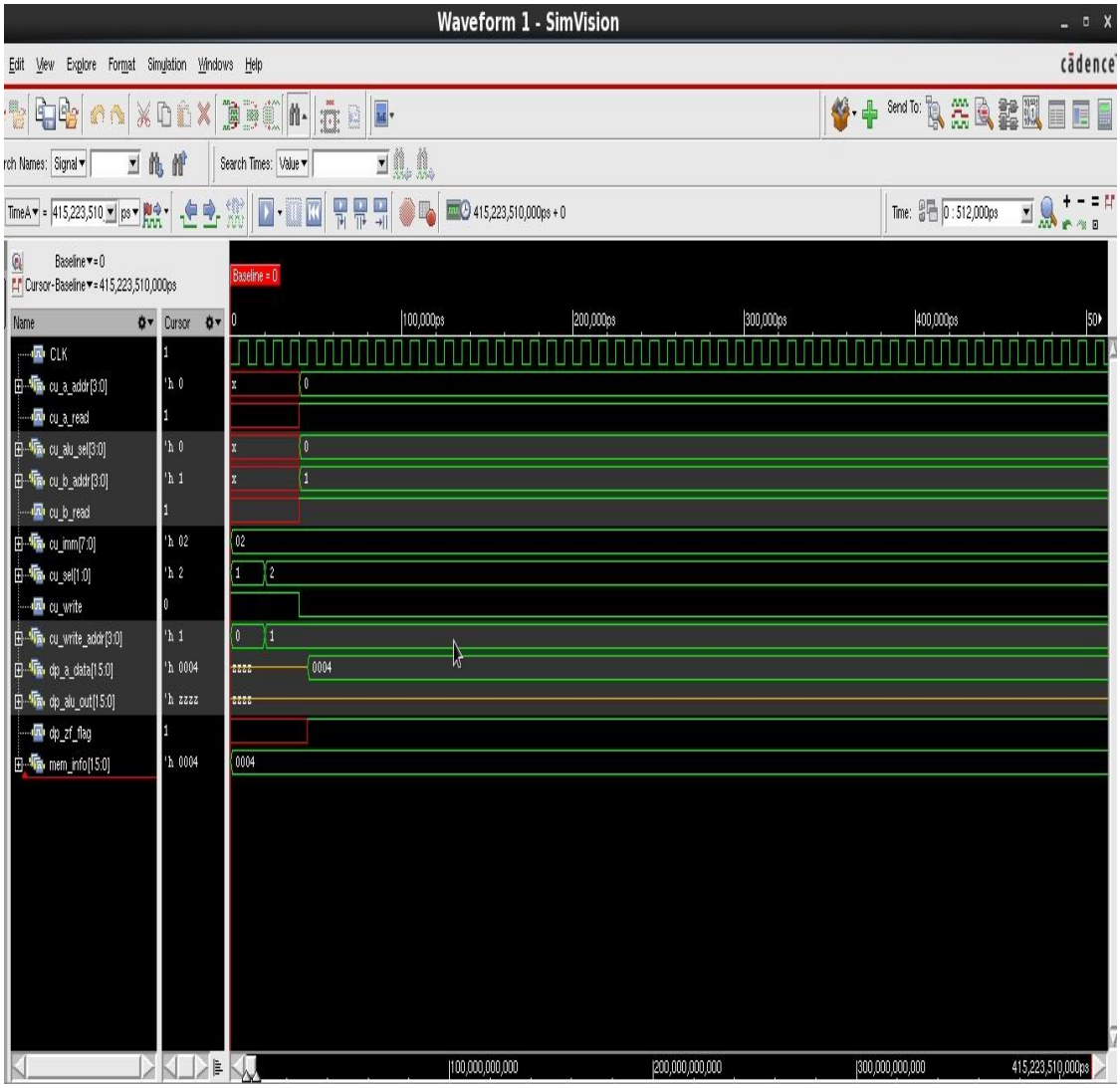

Fig 1: Simulation of Datapath

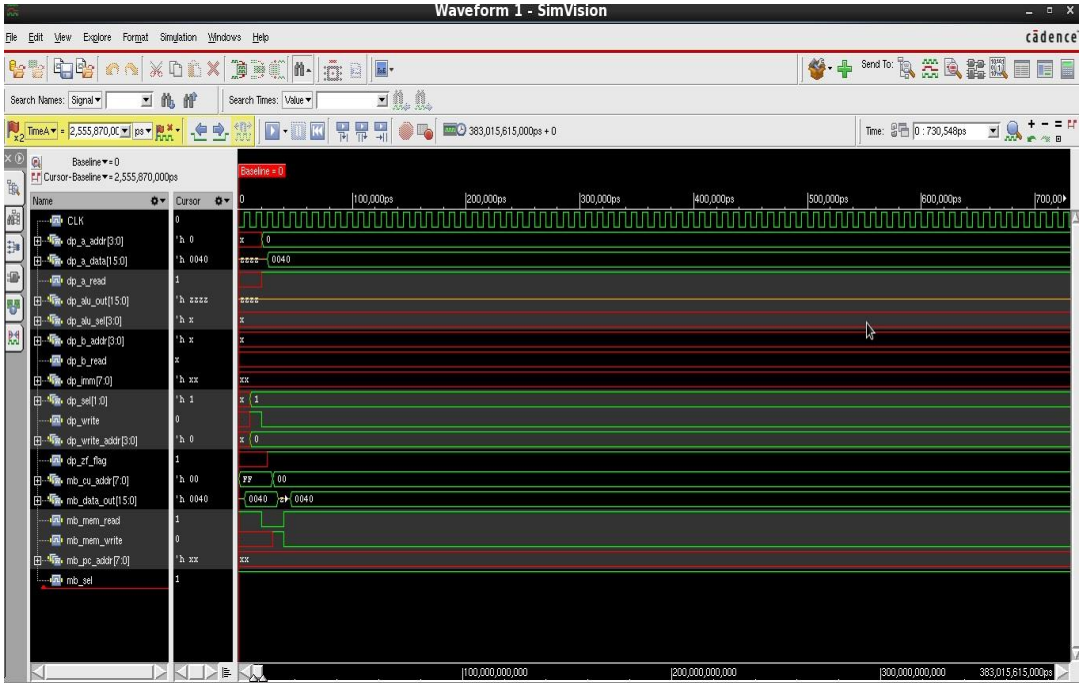

Fig 2: Simulation of Full Datapath

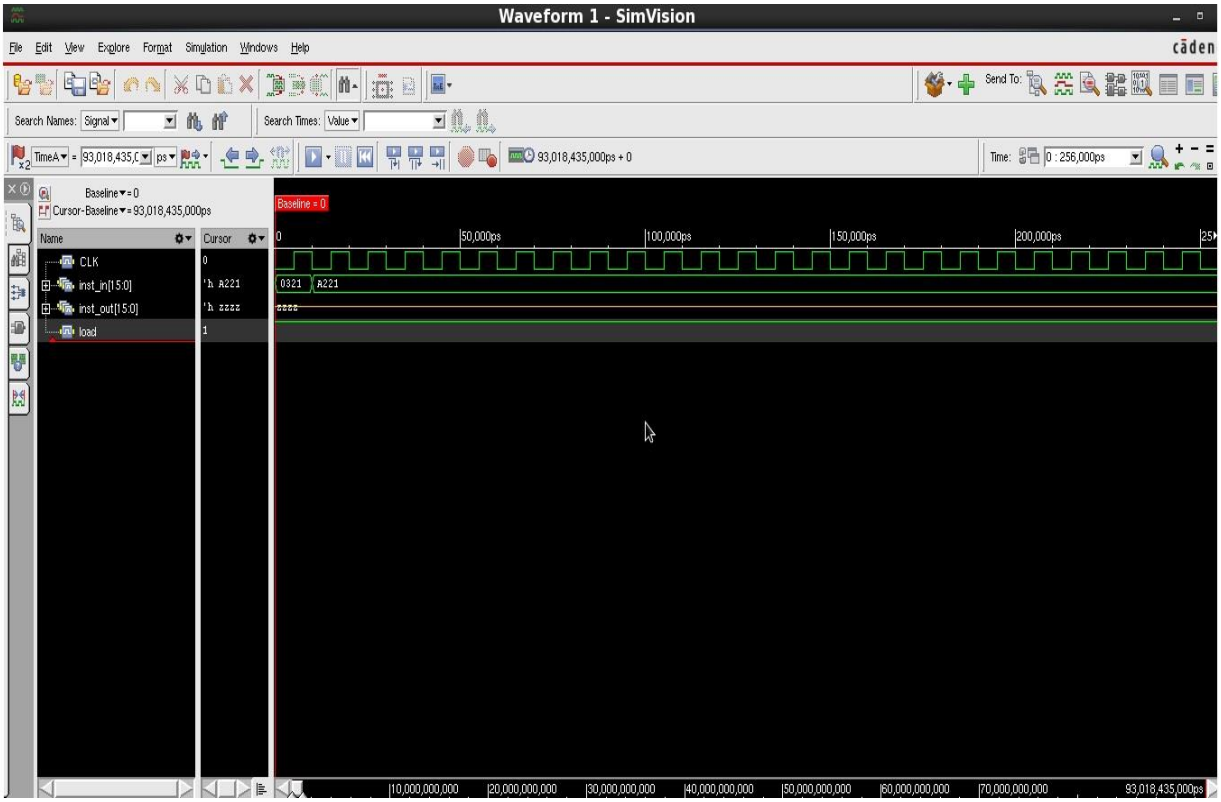

Fig 3: Simulation of IR

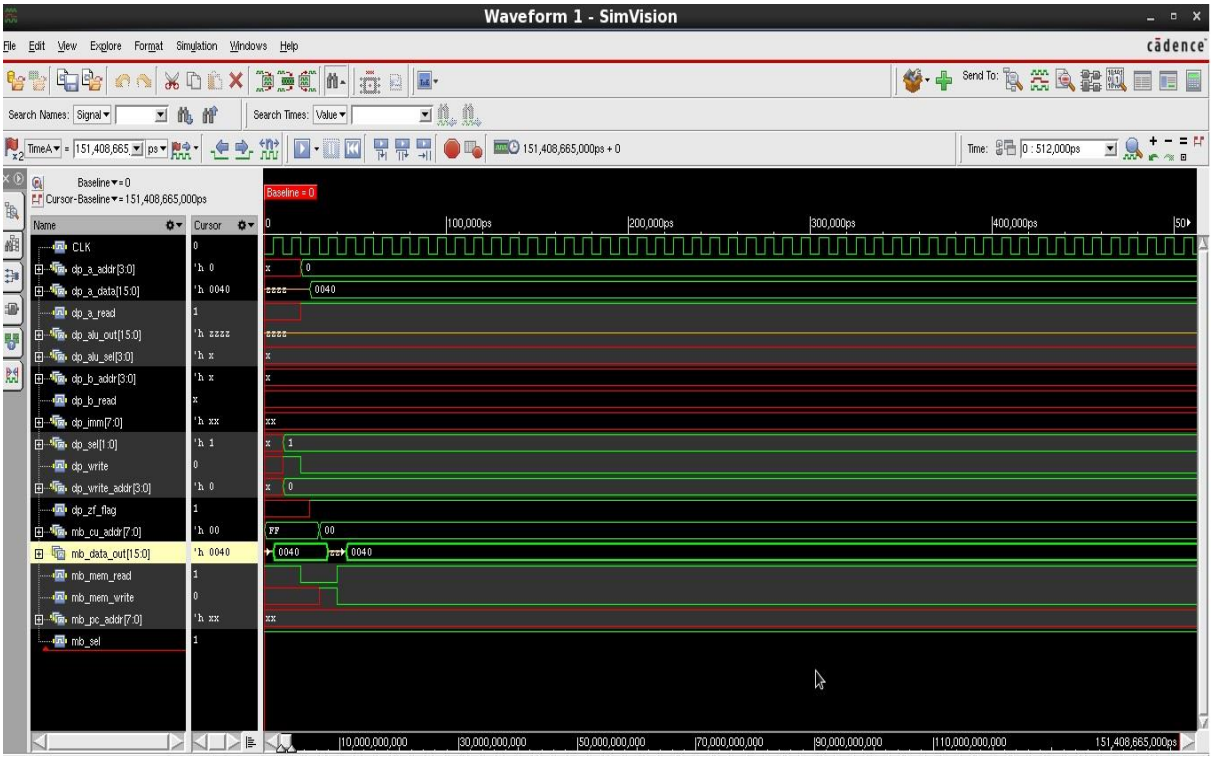

Fig 4 : Simulation of Mem_dp

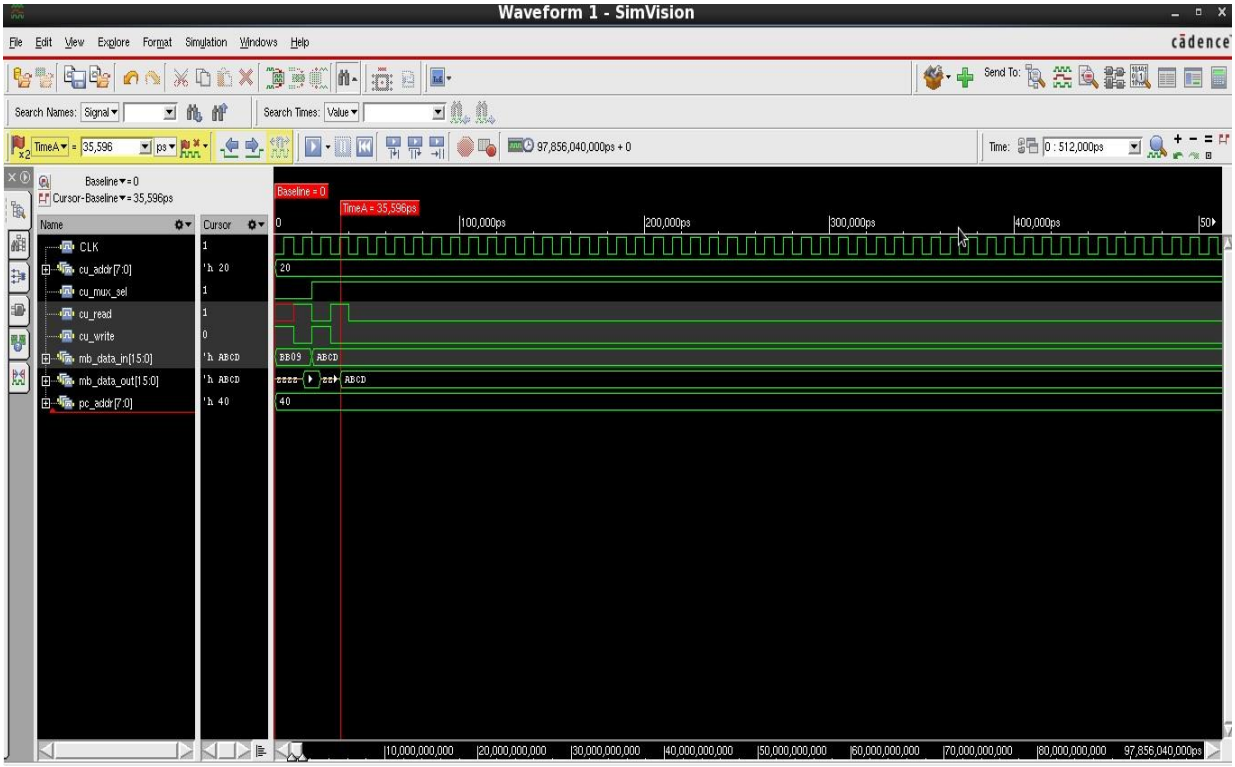

Fig 5: Simulation of Memory

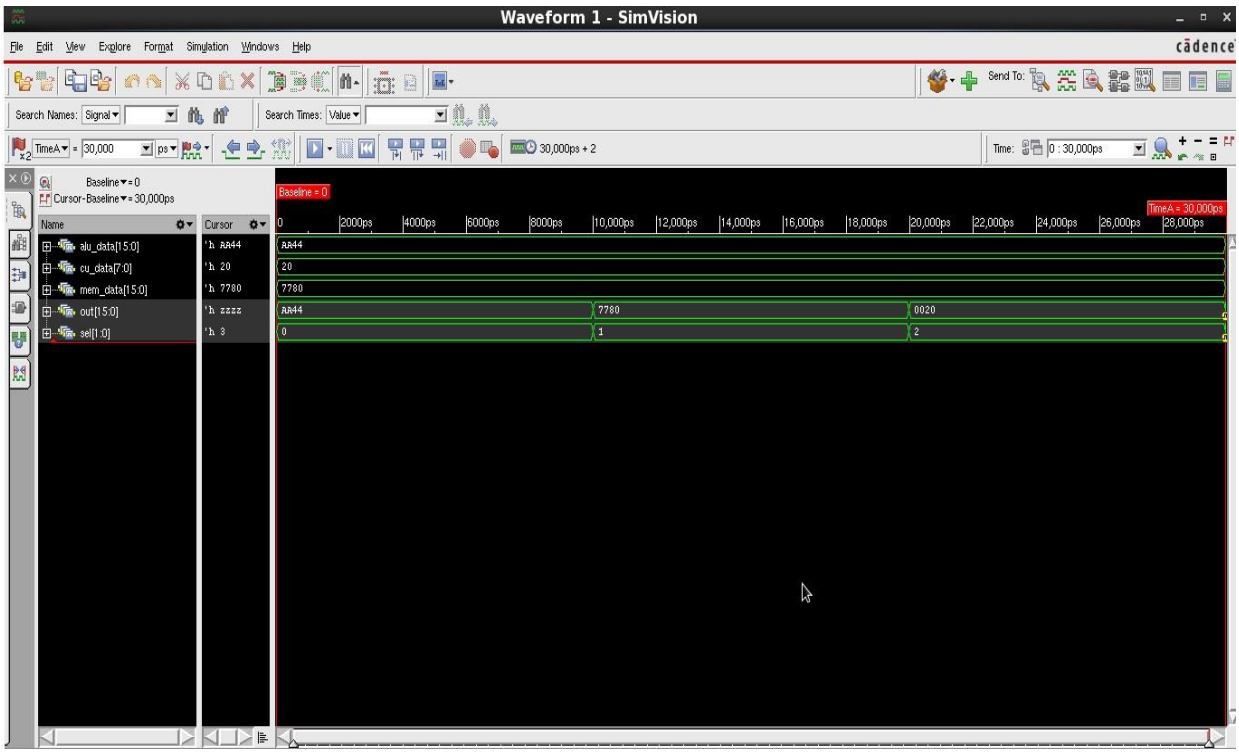

Fig 6: Simulation of Mux Data Path

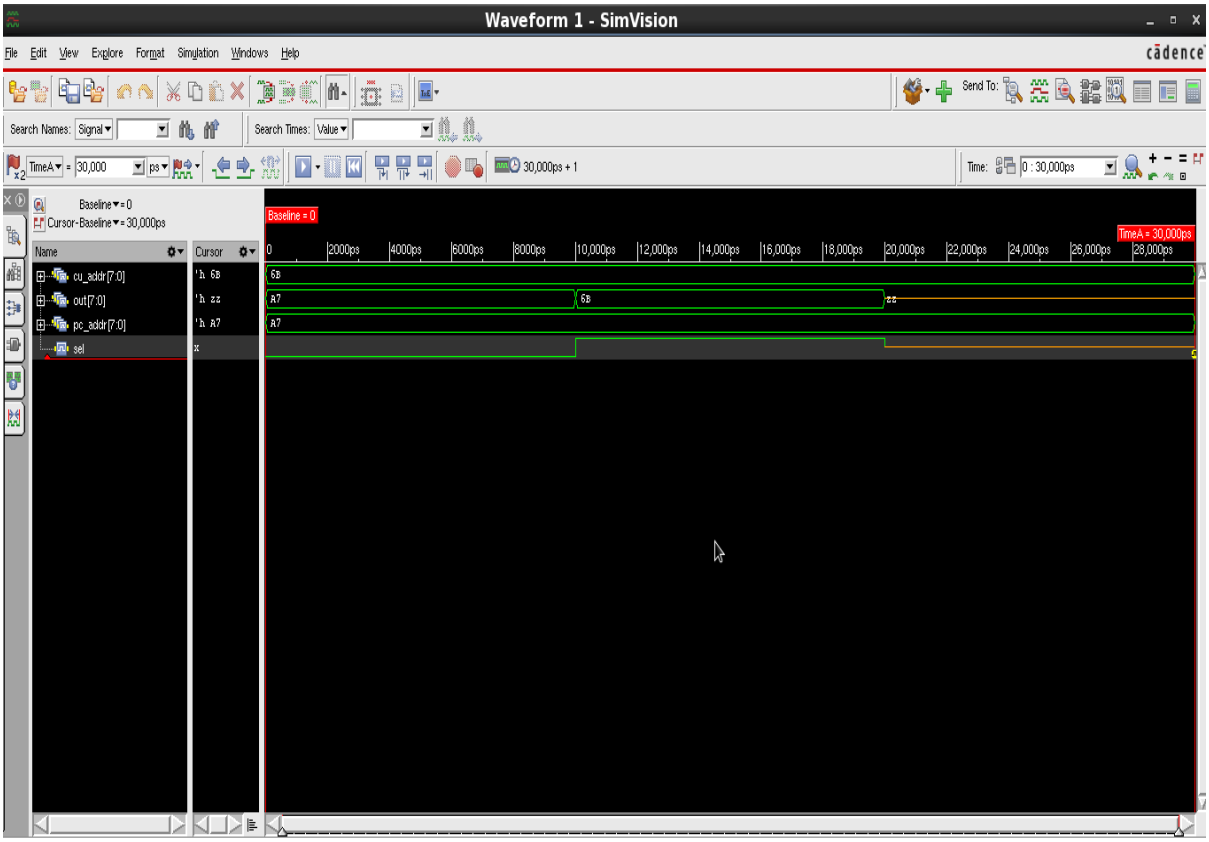

Fig 7 : Simulation of Mux Mem

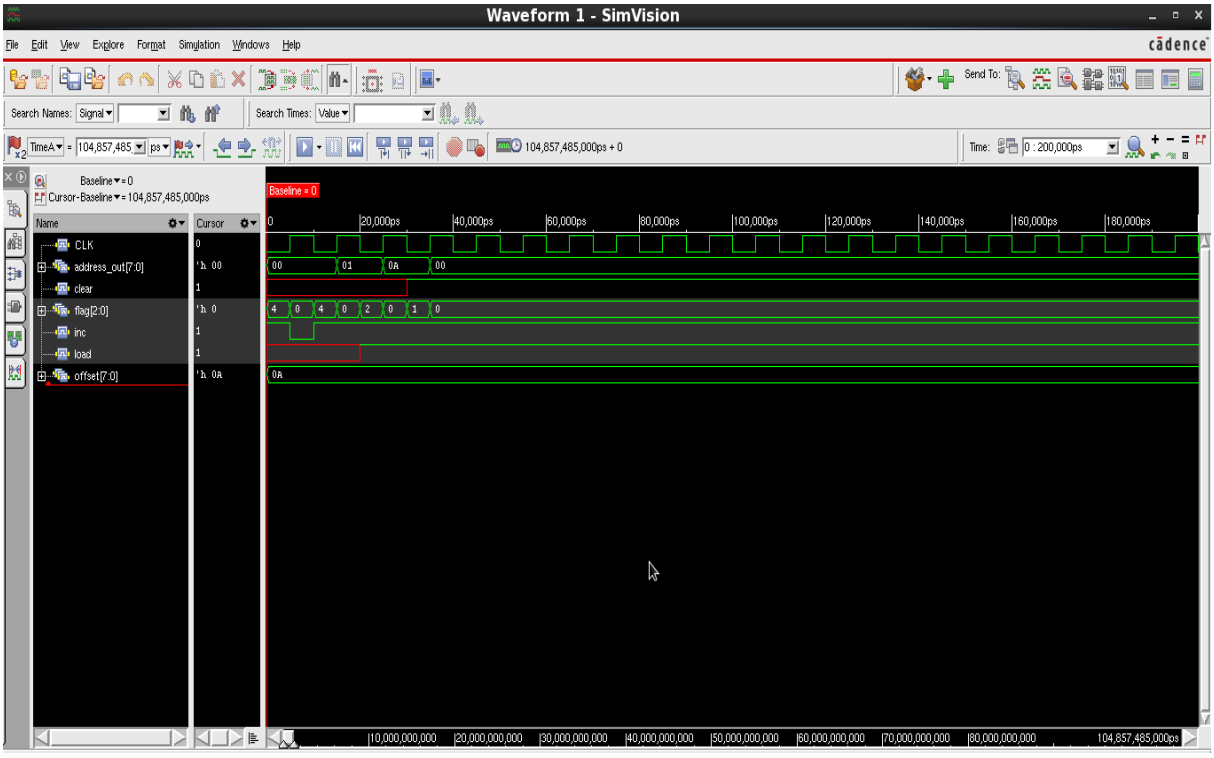

Fig 8 : Simulation of PC

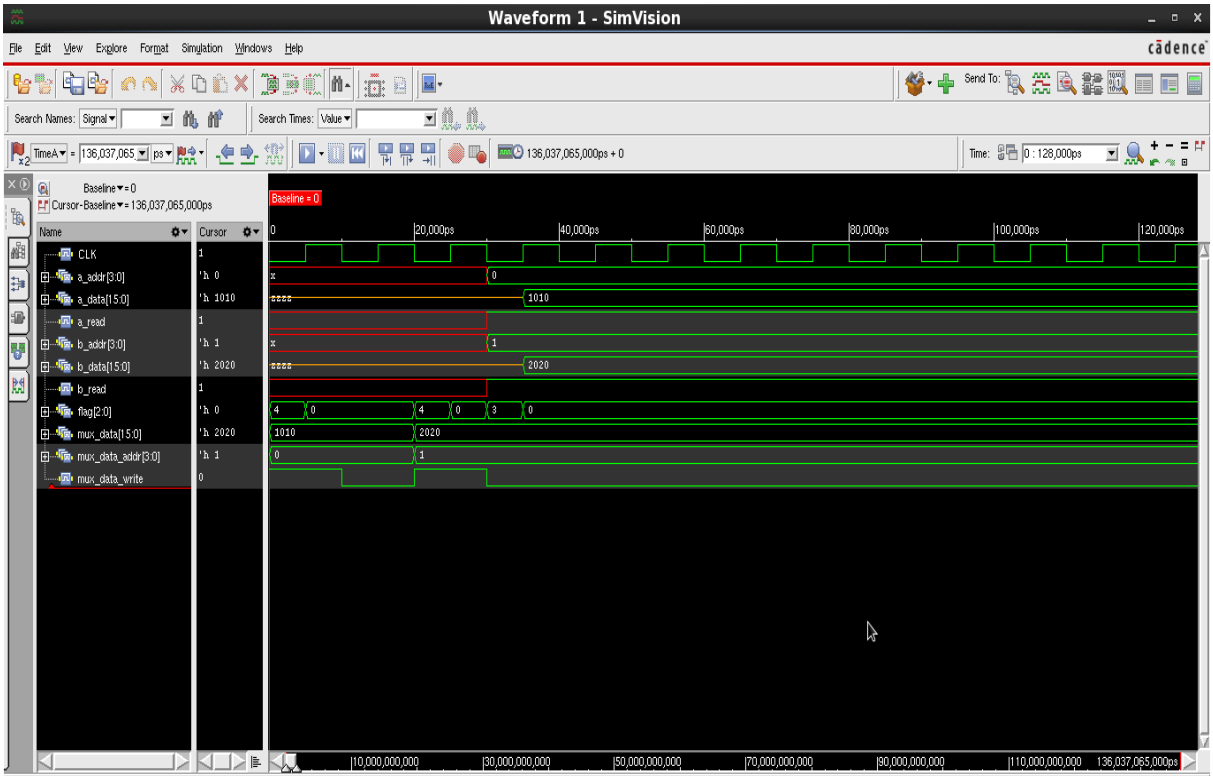

Fig 9 : Simulation of REG

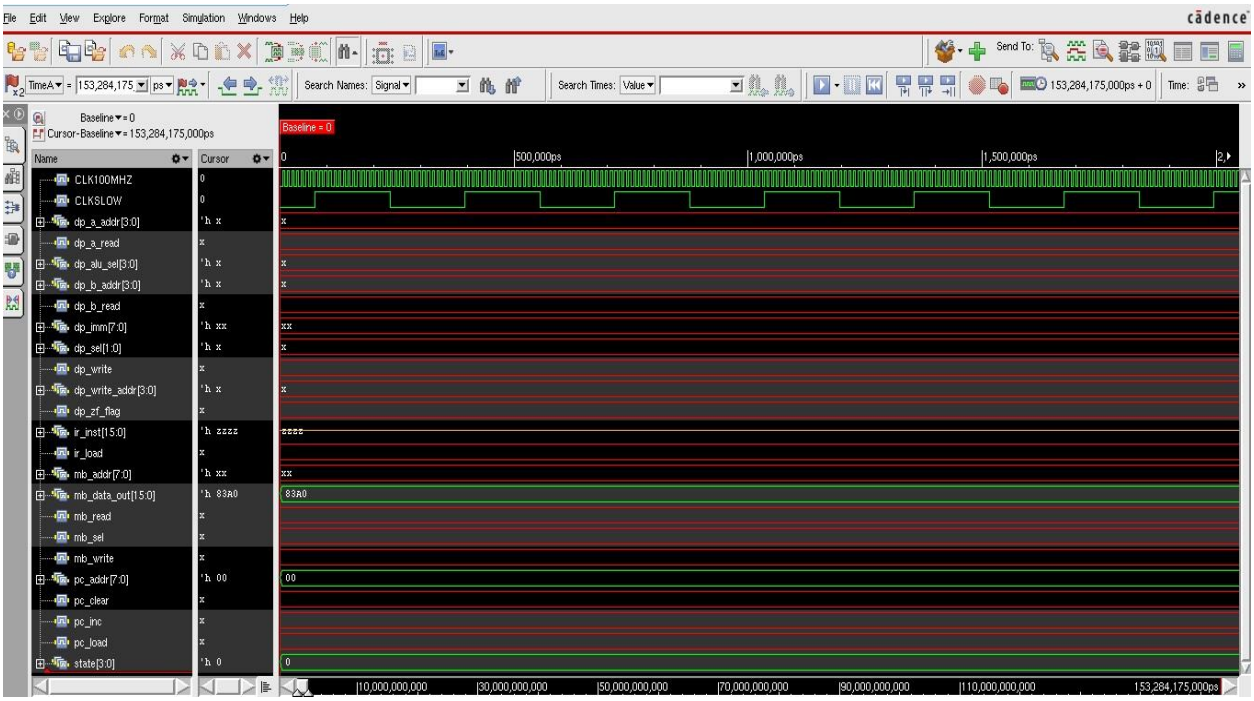

Fig 10: Simulation of cntrl_sim

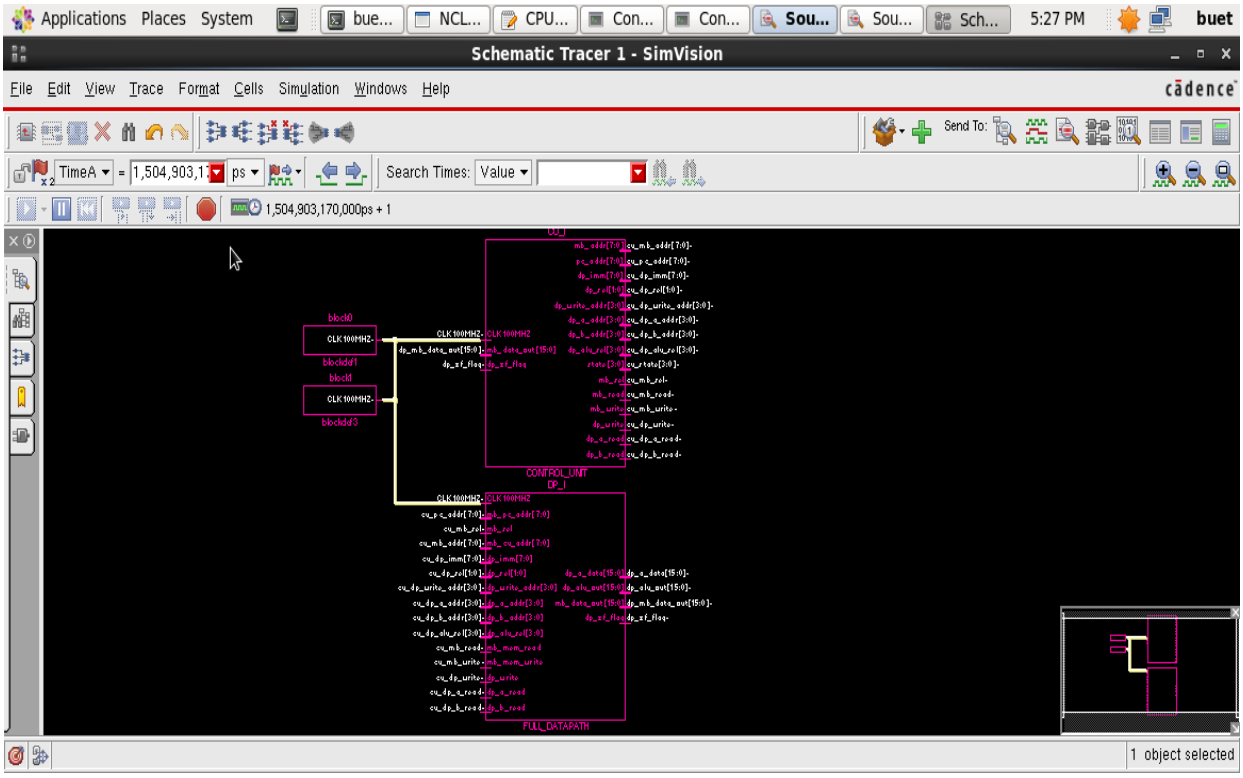

Fig 11: CPU Schematic

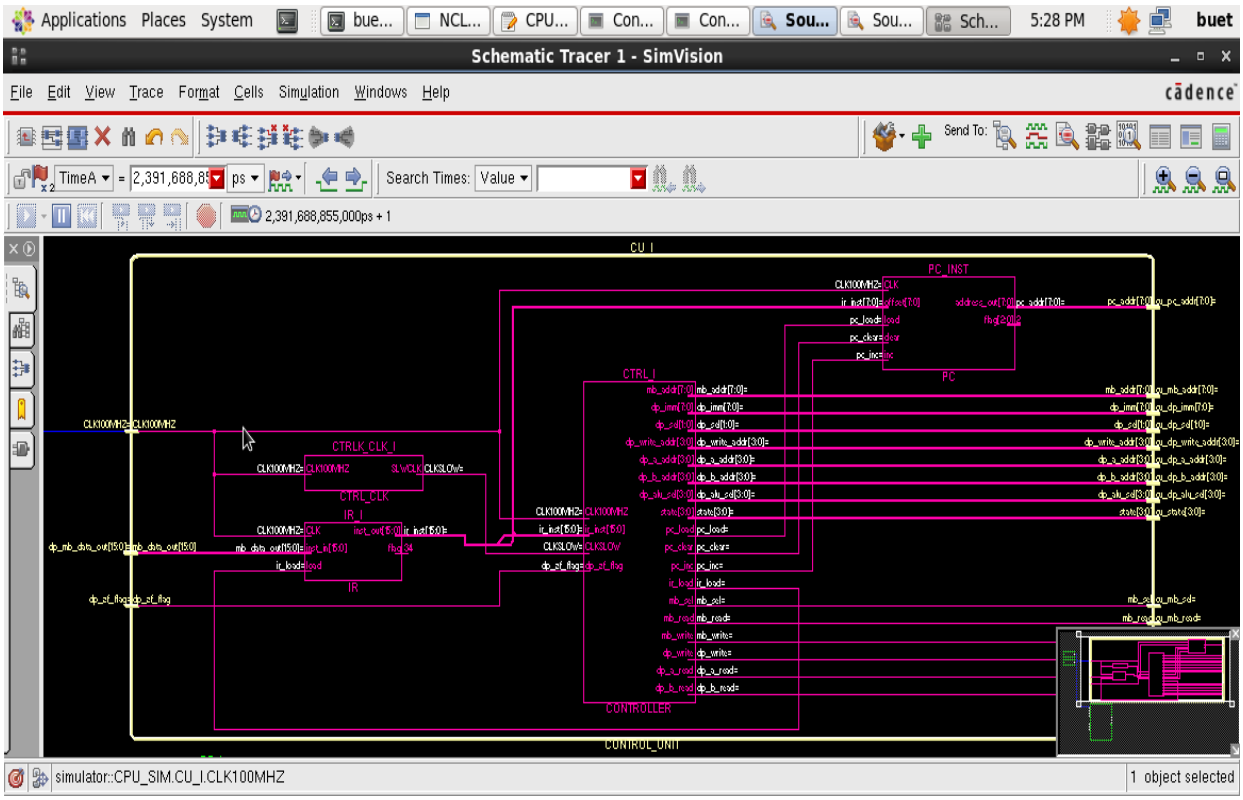

Fig 12: Internal Schematic of CPU

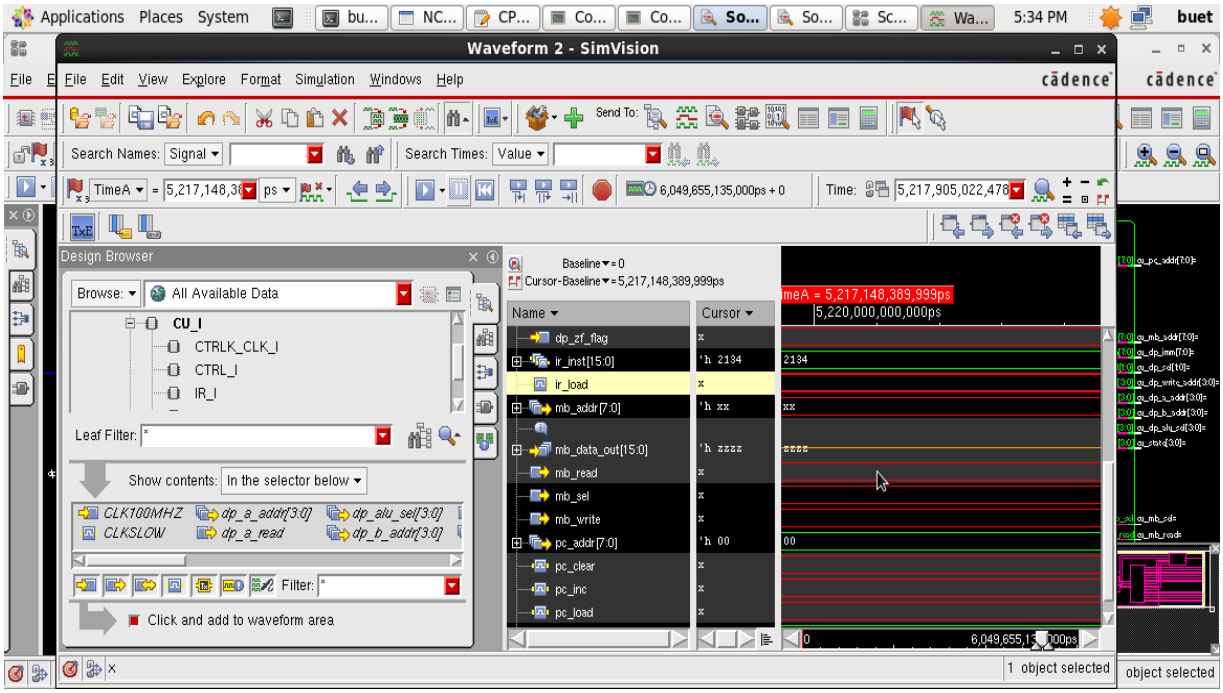

Fig 13: CPU Simulation waveform

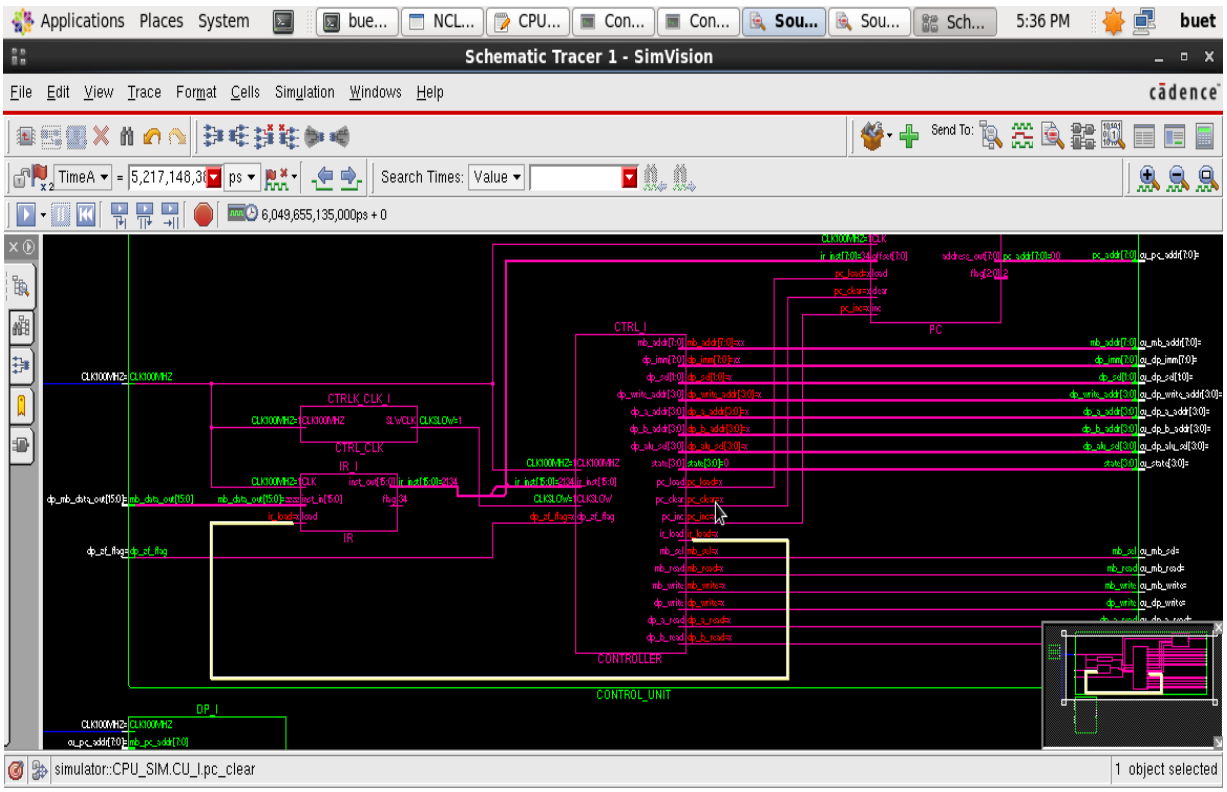

Fig 14: Basic Structure of proposed Design

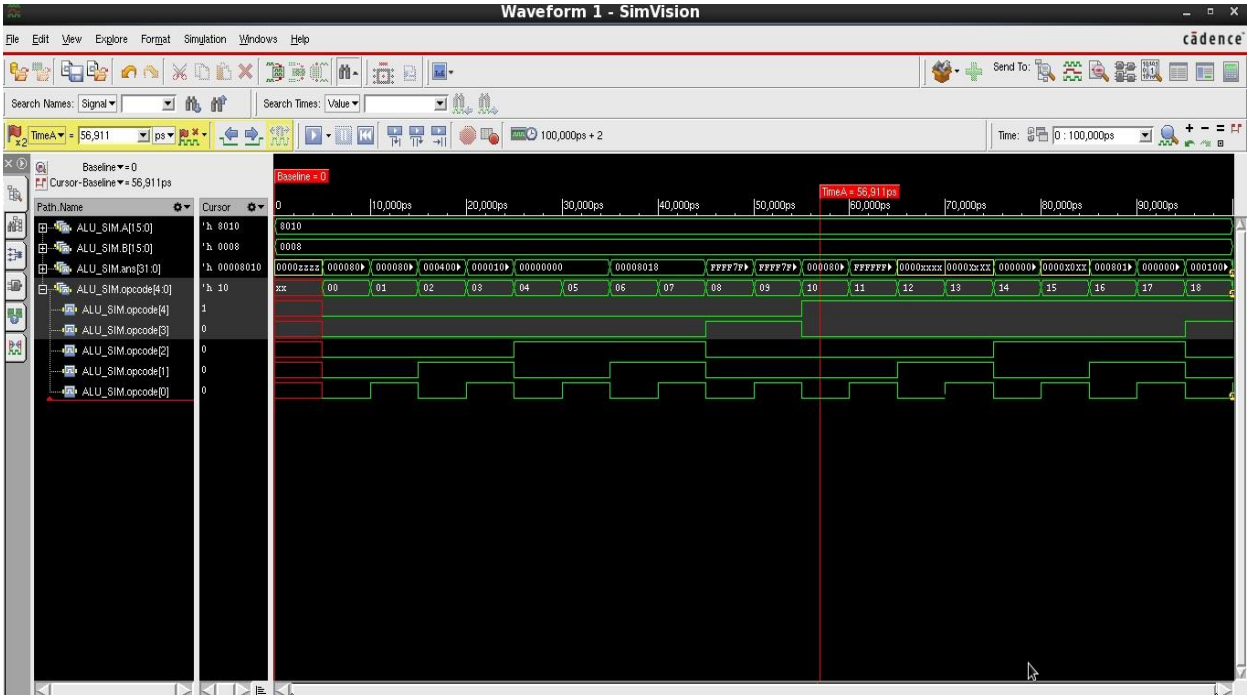

Fig 15: ALU simulation with opcodes

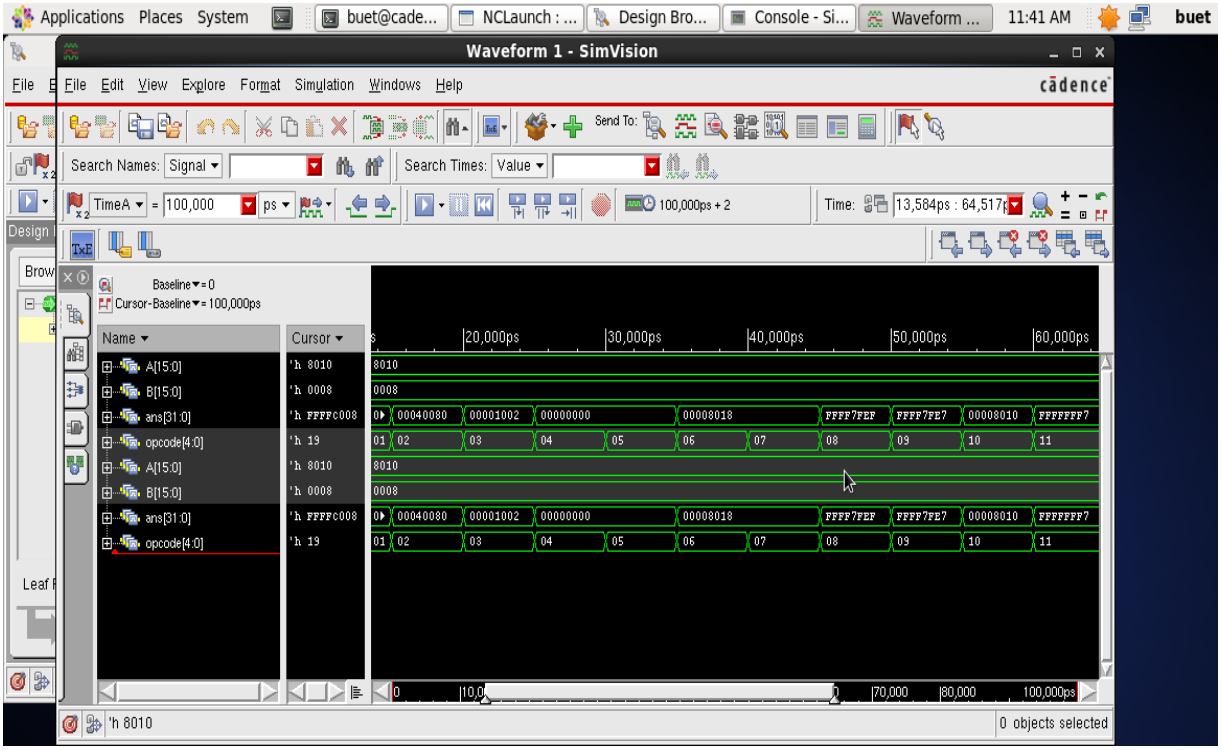

Fig 16: ALU simulation with opcodes with [15:0]A=8010 & [15:0]B=0008

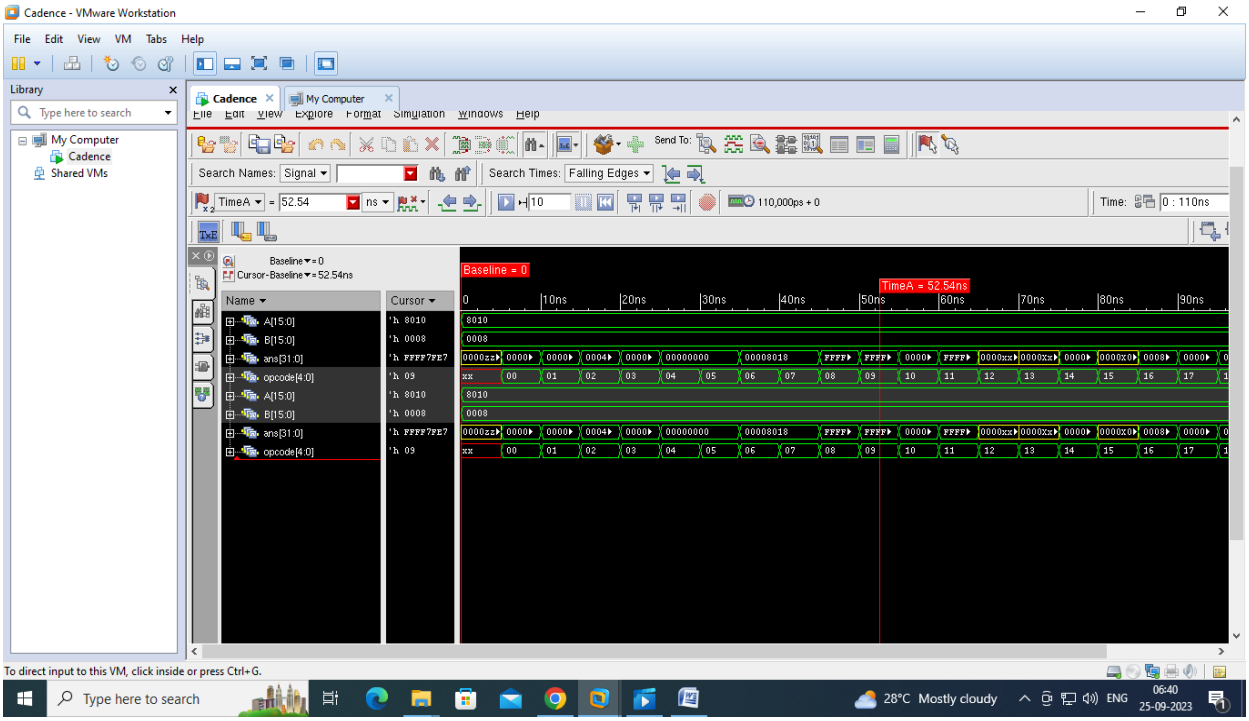

Fig 17: ALU simulation with opcodes with [15:0]A=8010 & [15:0]B=0008 contd…

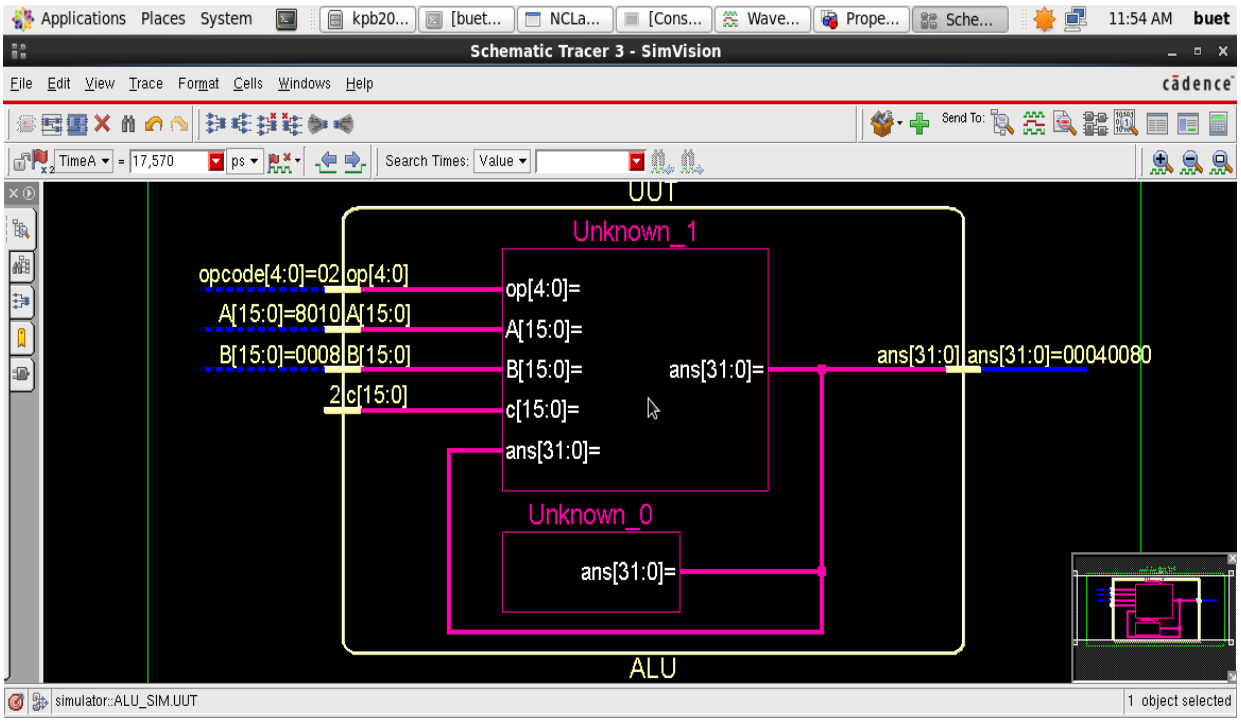

Fig 18: UUT of ALU

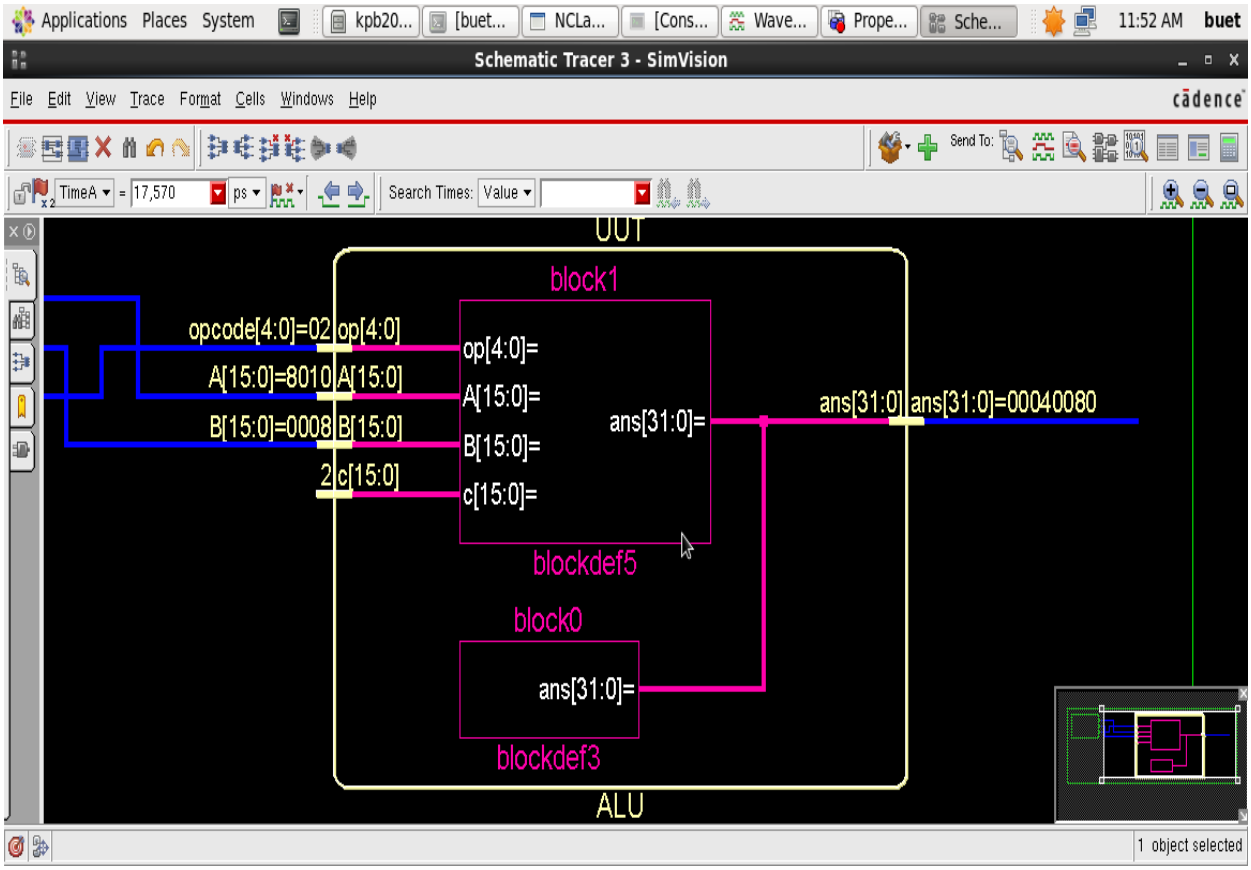

Fig 19: BLOCK UUT of ALU

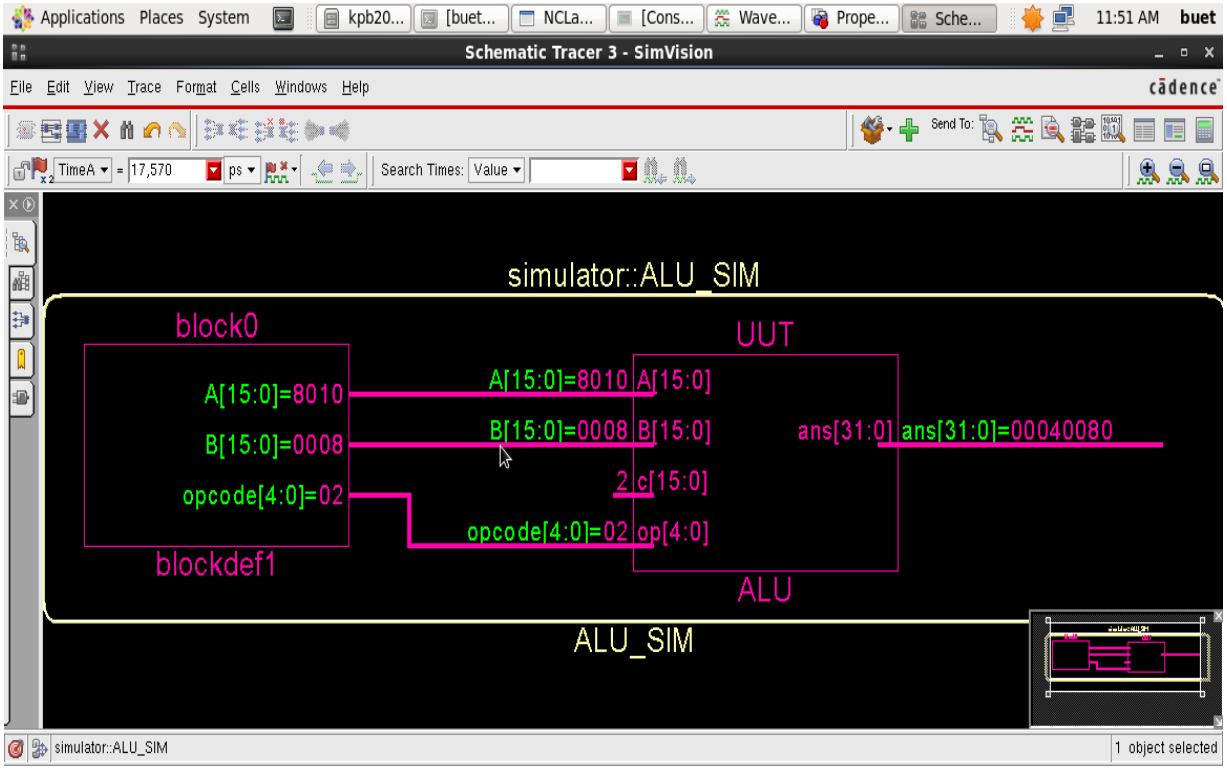

Fig 20: BLOCK SIMULATOR VIEW OF ALU

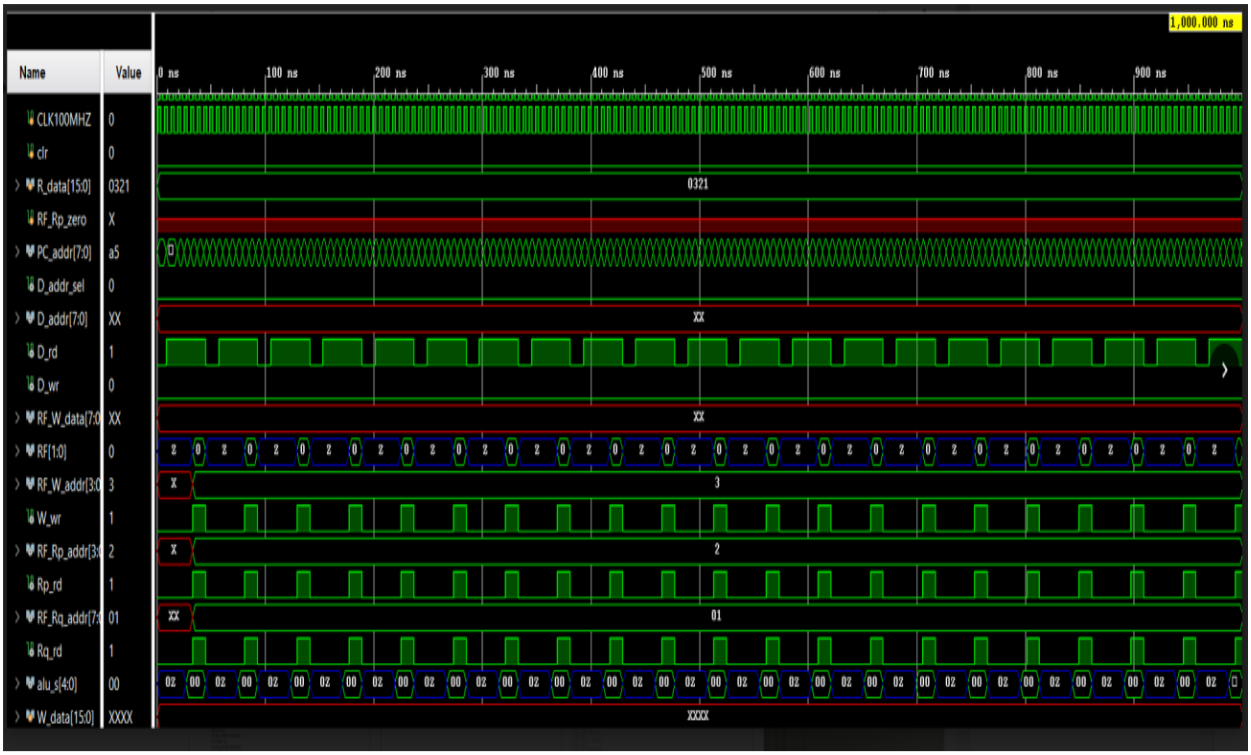

Fig 21: Add Instruction 0x0321 Control Signals From Control Unit

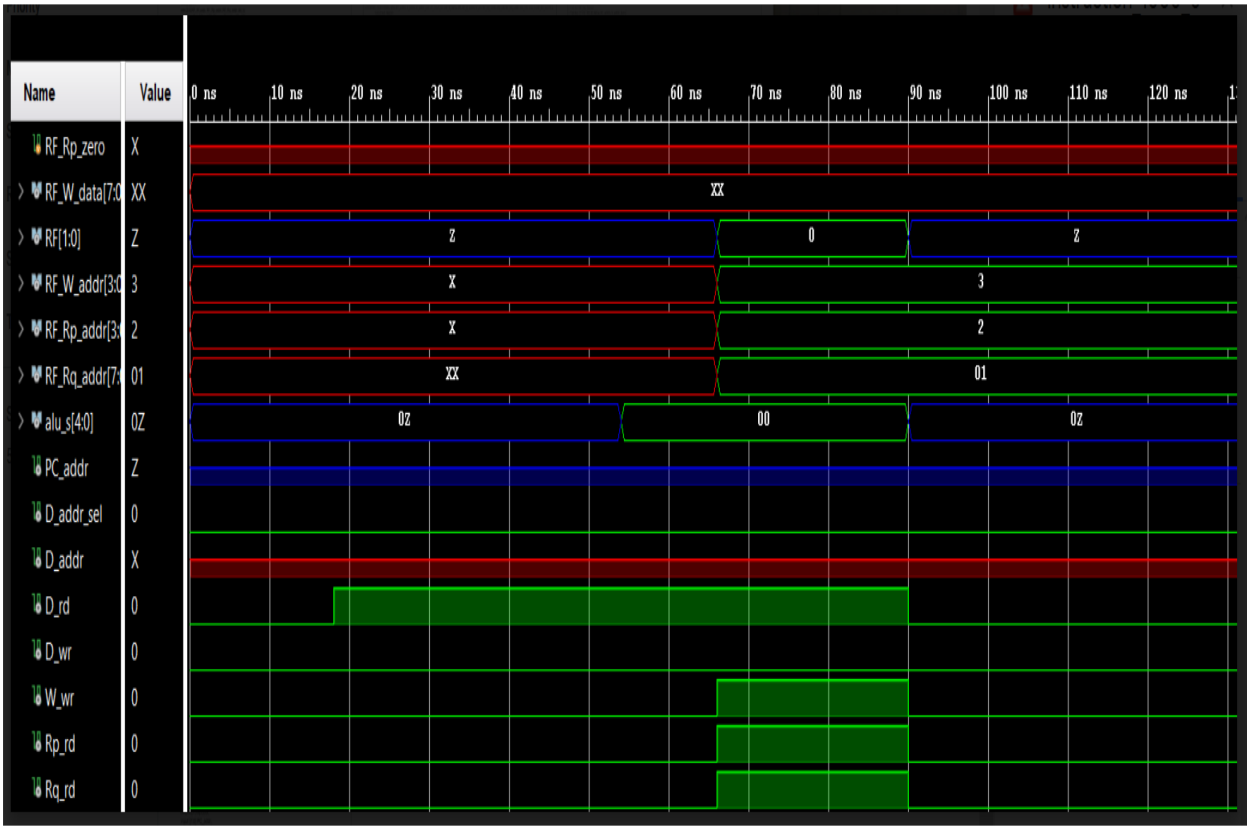

Fig 22: Add Instruction 0x0321 Control Signals From Control

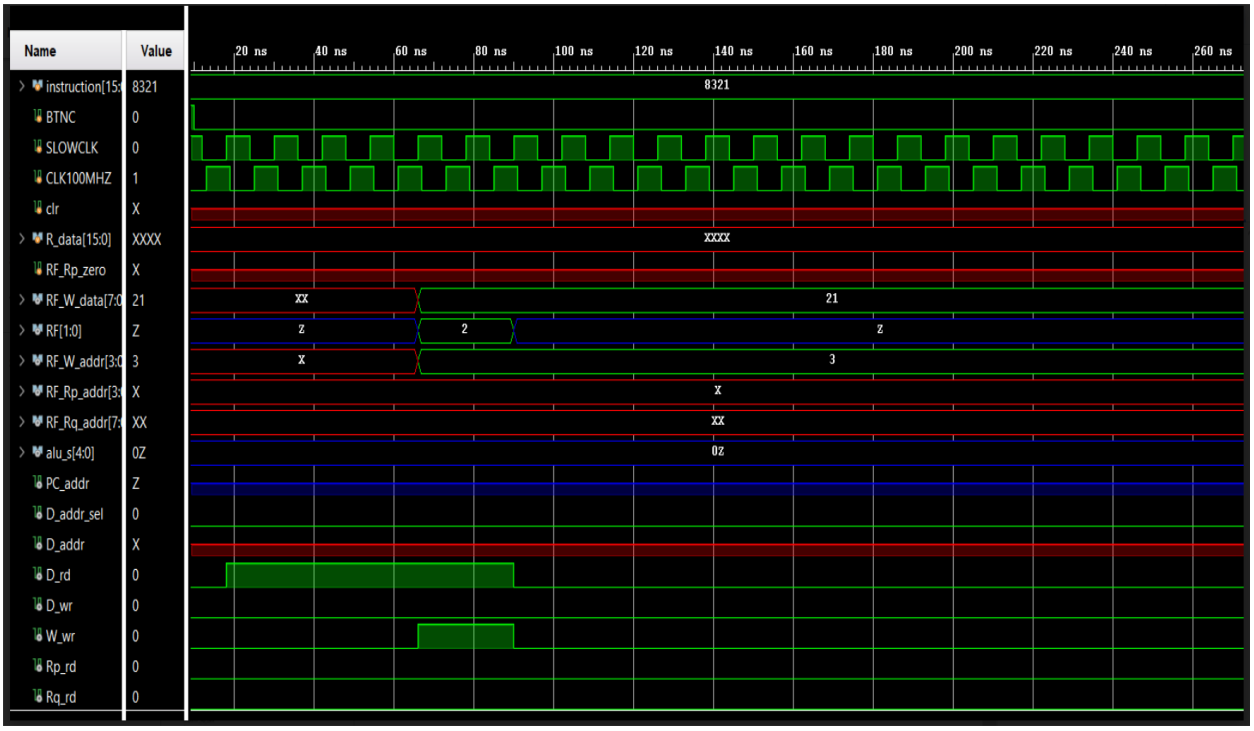

Fig 23: LI Instruction 0x8321 Control Signals From Control Unit

Fig 24: Entire CPU simulation with initial register and memory values

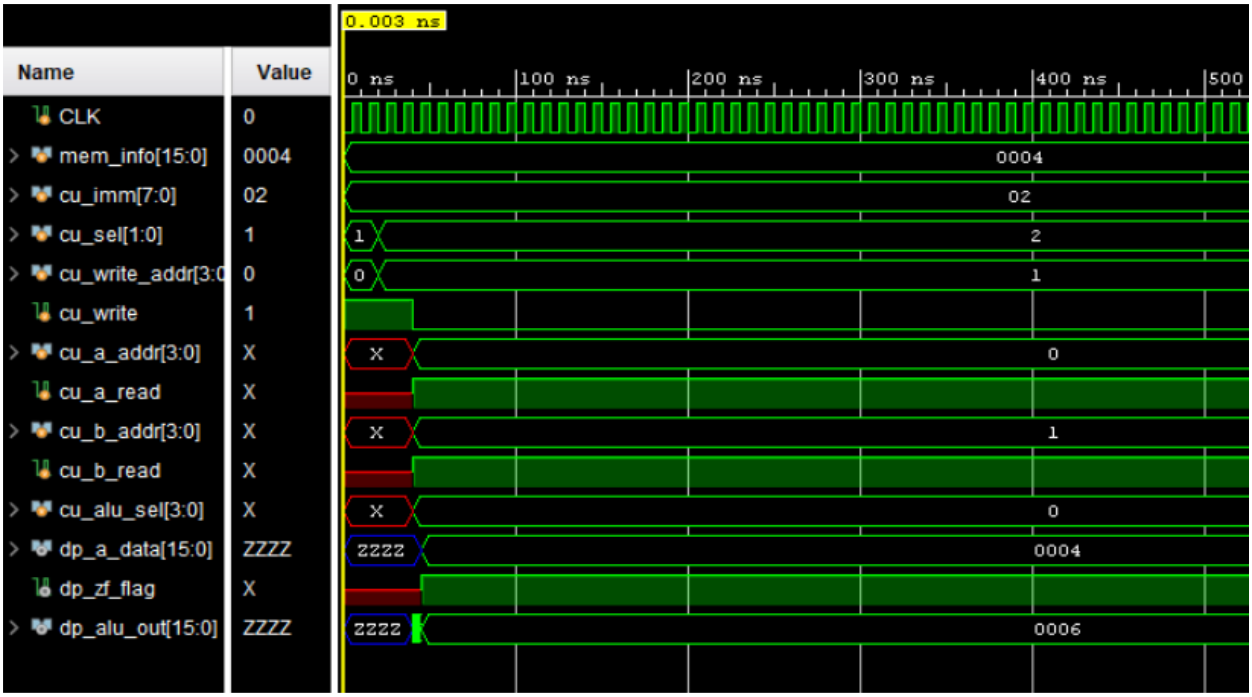

Fig 25: Datapath Simulation

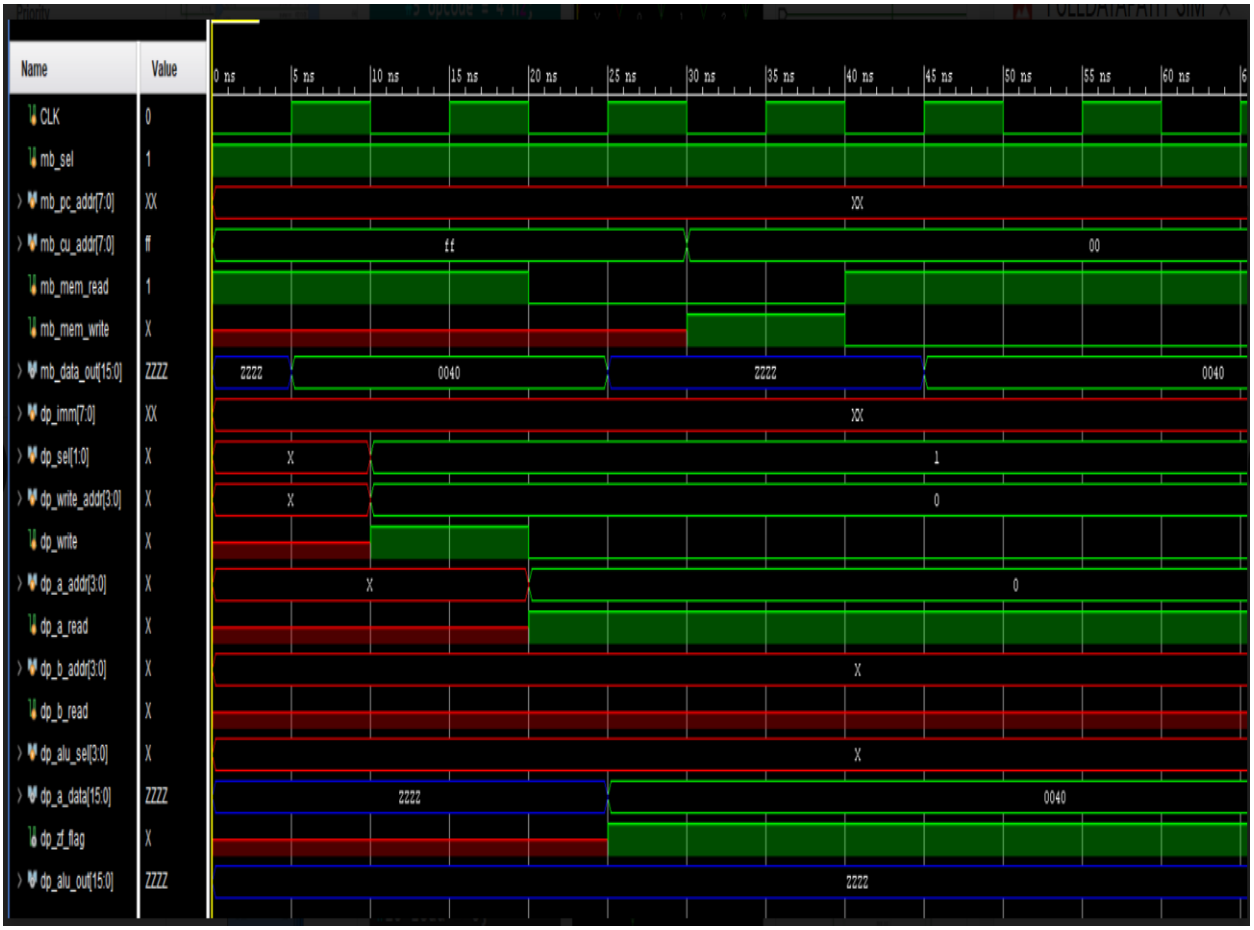

Fig 26: Memory and Datapath Simulation

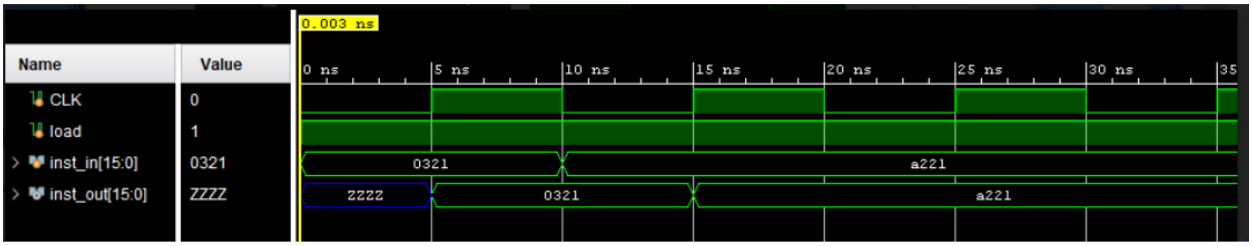

Fig 27: Instruction Register Simulation

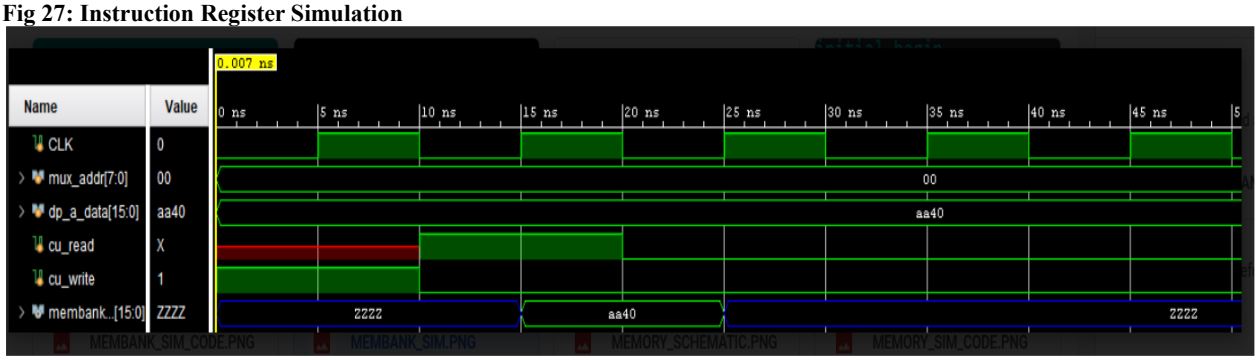

Fig 28: Memory bank Simulation

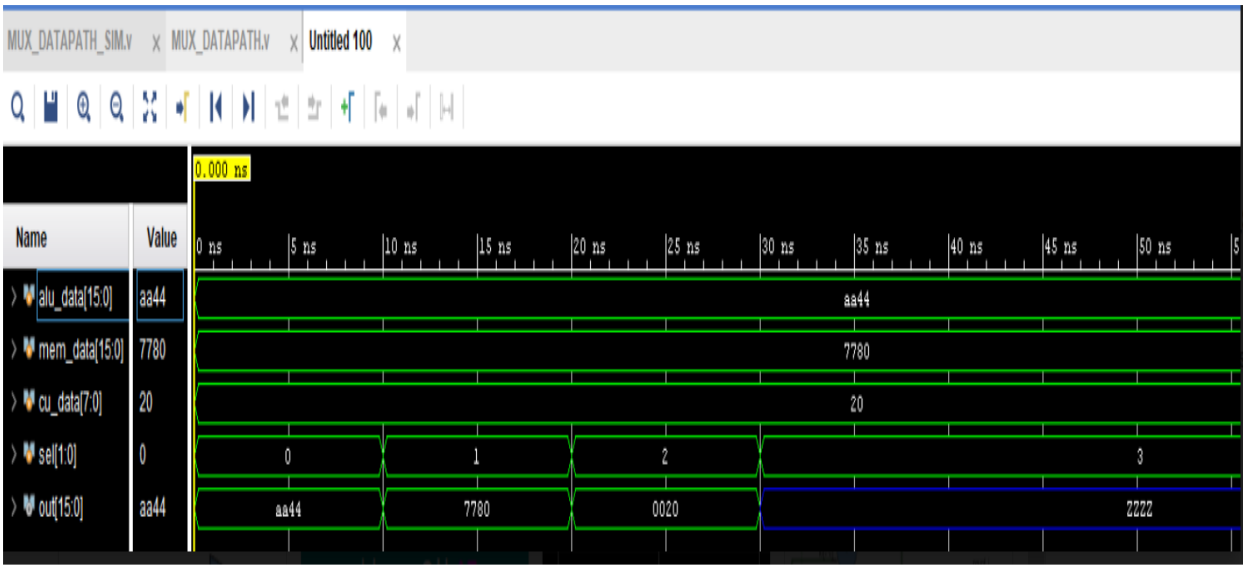

Fig 29: Memory Mux Simulation

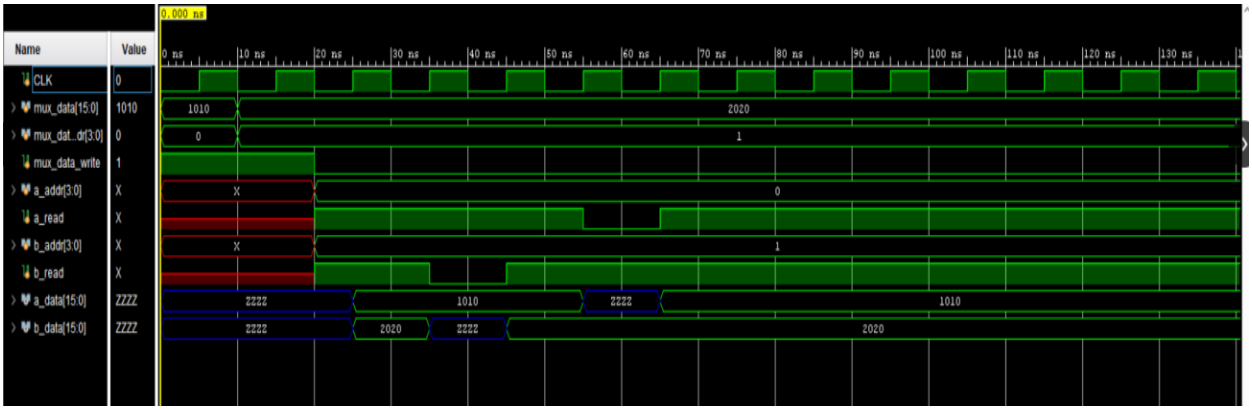

Fig 30: Reg bank Simulation

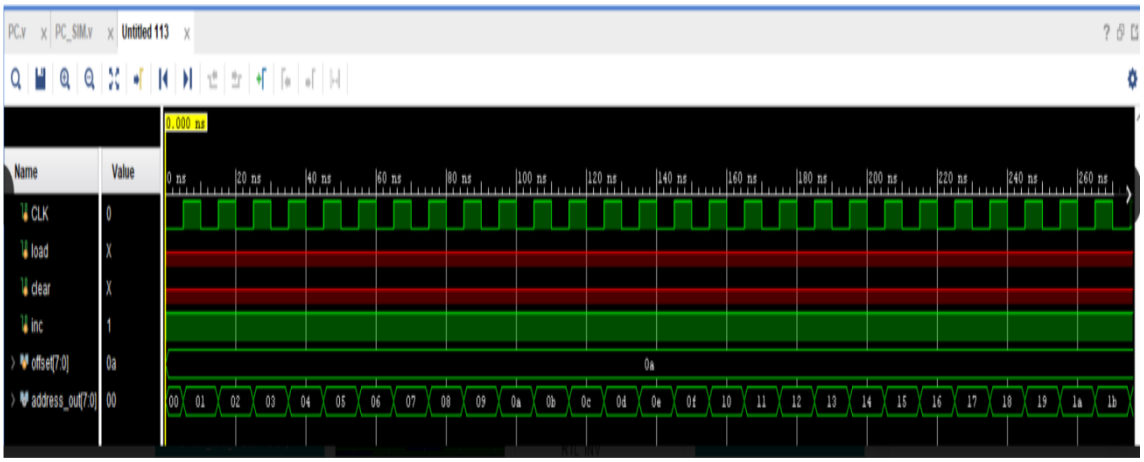

Fig 31: PC Bank Simulation

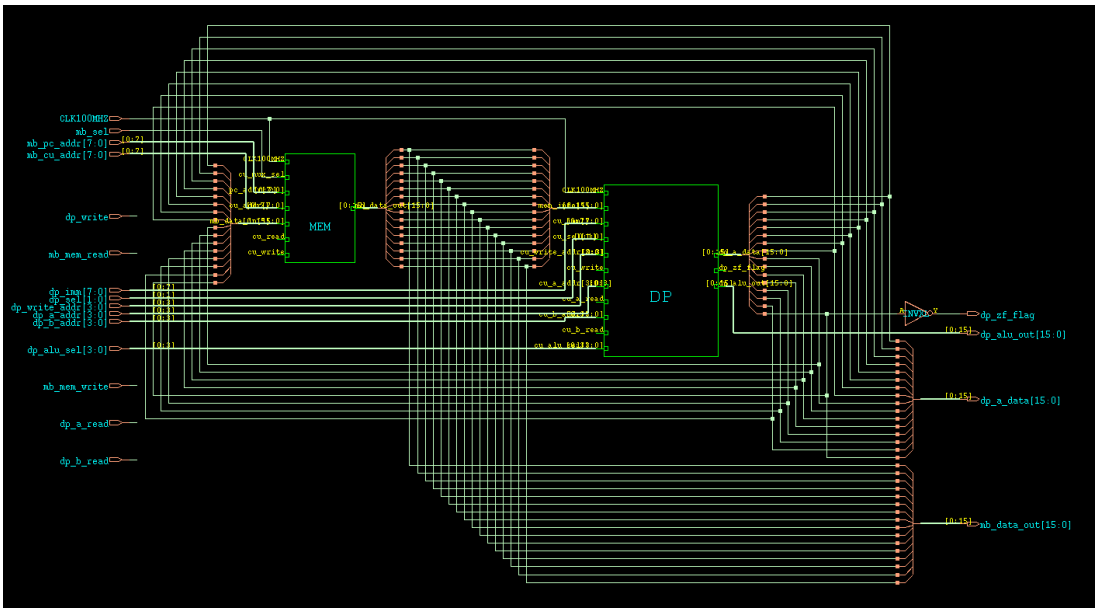

Fig 32: RTL view of Full datapath 90nm.

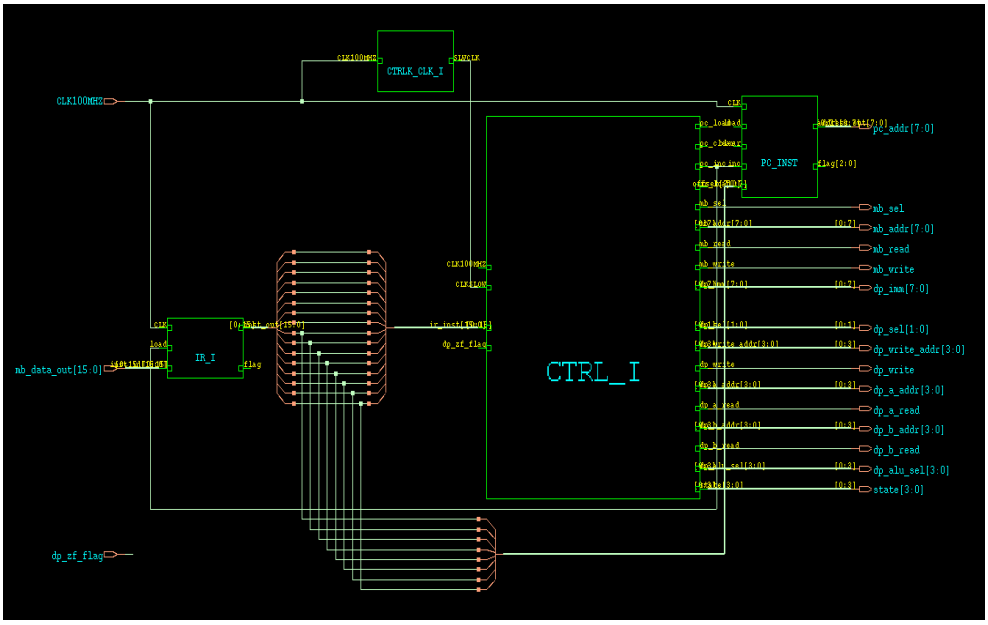

Fig 33: RTL view of Controller 90nm.

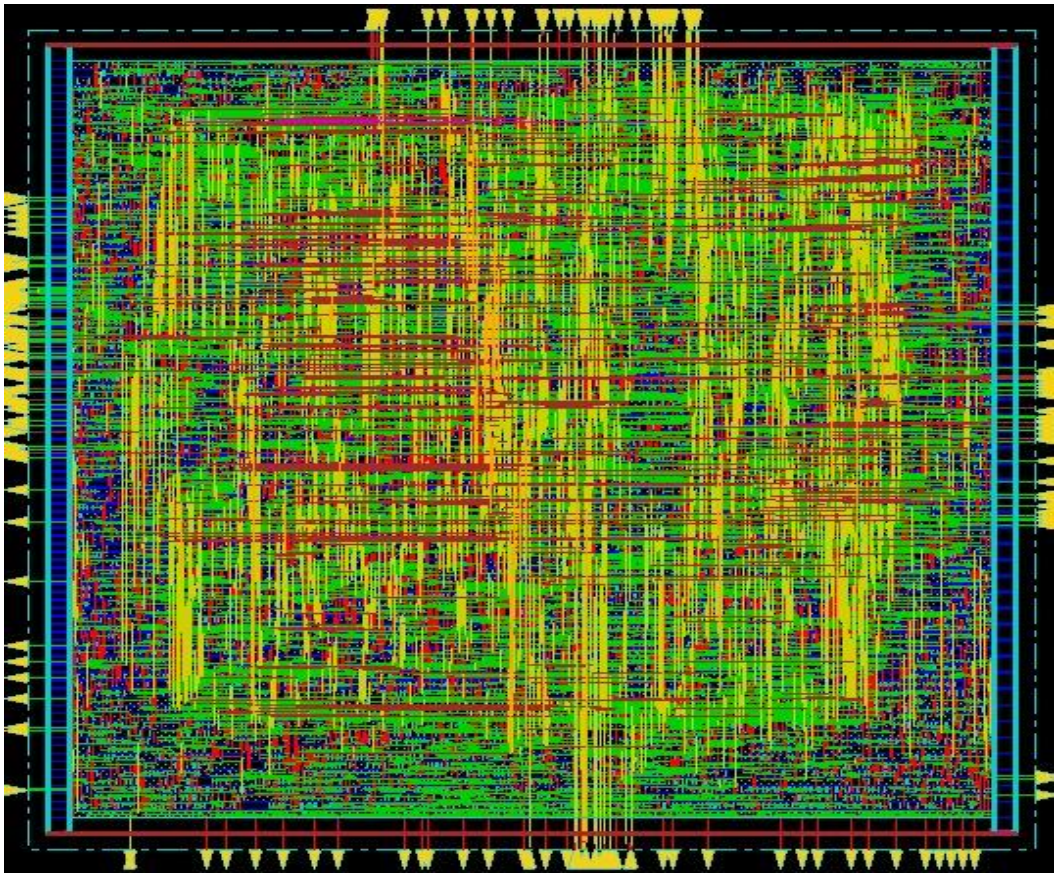

Fig 34: Physical layout

CONCLUSION

In this work power optimization technique CDC is used to reduce power consumption by selectively disabling the clock signal to specific parts of the circuit when they are not actively performing computations. This helps conserve power by preventing unnecessary switching activity in idle or non-operational regions of the design. Analyzing clock domain interactions and clock domain crossing issues using Genus is done in this work. Optimization of clock domain architectures to minimize power consumption is encountered successfully. Comprehensive clock domain crossing analysis to identify and resolve clock domain crossing issues is done. Sequential and combinational optimizations to reduce power consumption using restructuring logic, retiming, and area-based optimization is made in this work. Explicitly insertion of clock gating cells in critical paths where the clock can be gated during inactive periods is compelled in this work.
The full-data-path analysis using 90nm are depicted in below figure reports figures 34,35,36,37.

```
|=============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023   10:43:56 am
  Module:                 FULL_DATAPATH
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

   Instance      Module     Cell Count  Cell Area  Net Area   Total Area  Wireload
-------------------------------------------------------------------------------------
FULL_DATAPATH                19052 125516.727     0.000   125516.727    <none> (D)
  MEM         MEMORY         16042 103964.756     0.000   103964.756    <none> (D)
    MEMBANK_I MEMBANK        16034 103910.260     0.000   103910.260    <none> (D)
  DP          DATAPATH        3009  21549.700     0.000    21549.700    <none> (D)
    ALU_I     ALU             1393  11080.259     0.000    11080.259    <none> (D)
    REGBANK_I REGBANK         1556  10025.897     0.000    10025.897    <none> (D)
    MUX_I     MUX_DATAPATH      53    411.754     0.000      411.754    <none> (D)

 (D) = wireload is default in technology library
```

Fig 34: 90nm Genus FD Area report

```
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023   10:43:55 am
  Module:                 FULL_DATAPATH
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

                      Leakage     Dynamic        Total
   Instance   Cells  Power(nW)   Power(nW)     Power(nW)
-------------------------------------------------------------
FULL_DATAPATH 19052 623180.960  861963.26963 1478912.42111
  MEM         16042  51886.566  962211.23945  962212.48931
    MEMBANK_I 16034  51843.106  962201.61526  962201.93633
  DP           3009 104306.636  646778.41941  647821.48578
    REGBANK_I  1556  54427.732  540010.58393  540554.86125
    ALU_I      1393  47267.739  103197.85030  103670.52769
    MUX_I        53   2322.131     561.17624     584.39755
```

Fig 35: 90nm Genus FD power report

```
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023 10:43:56 am
  Module:                 FULL_DATAPATH
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================


Path 1: VIOLATED (-1392 ps) Setup Check with Pin MEM/MEMBANK_I/data_out_reg[14]/CK->D
          Group: CLK100MHZ
     Startpoint: (R) DP/REGBANK_I/a_data_reg[14]/CK
          Clock: (R) CLK100MHZ
       Endpoint: (F) MEM/MEMBANK_I/data_out_reg[14]/D
          Clock: (R) CLK100MHZ

                     Capture       Launch
       Clock Edge:+      100            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     100            0

             Setup:-      80
       Uncertainty:-      10
     Required Time:=      10
      Launch Clock:-       0
         Data Path:-    1402
             Slack:=   -1392
```

Timing Point	Flags	Arc	Edge	Cell	Fanout	Load (fF)	Trans (ps)	Delay (ps)	Arrival (ps)	Instance Location
DP/REGBANK_I/a_data_reg[14]/CK	-	-	R	(arrival)	3603	-	100	-	0	(-,-)
DP/REGBANK_I/a_data_reg[14]/Q	-	CK->Q	F	DFFQX4	3	43.3	99	412	412	(-,-)
MEM/MEMBANK_I/fopt395710/Y	-	A->Y	R	INVX16	8	113.2	77	81	493	(-,-)
MEM/MEMBANK_I/fopt395673/Y	-	A->Y	F	INVX12	9	41.7	43	46	539	(-,-)
MEM/MEMBANK_I/fopt395663/Y	-	A->Y	R	INVX3	5	16.0	52	56	594	(-,-)
MEM/MEMBANK_I/fopt395662/Y	-	A->Y	F	CLKINVX2	5	10.2	45	48	642	(-,-)
MEM/MEMBANK_I/fopt395658/Y	-	A->Y	R	INVX1	2	5.4	55	58	700	(-,-)
MEM/MEMBANK_I/g388444/Y	-	A1->Y	F	OAI21X1	2	4.2	144	83	783	(-,-)
MEM/MEMBANK_I/g381375/Y	-	A0->Y	R	AOI221X1	1	2.8	191	194	977	(-,-)
MEM/MEMBANK_I/g381321/Y	-	B->Y	F	NAND2X1	1	2.8	93	86	1063	(-,-)
MEM/MEMBANK_I/g381309/Y	-	C->Y	R	NOR3X1	1	1.8	99	94	1157	(-,-)
MEM/MEMBANK_I/g381297/Y	-	AN->Y	R	NOR3BX1	1	2.7	128	182	1339	(-,-)
MEM/MEMBANK_I/g381261/Y	-	A->Y	F	NAND2X1	1	1.6	59	64	1402	(-,-)
MEM/MEMBANK_I/data_out_reg[14]/D <<<	-		F	DFFQX1	1	-	-	0	1402	(-,-)

Fig 36: 90nm Genus FD timing report

```
------------------------------------------------------------
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023   10:43:56 am
  Module:                 FULL_DATAPATH
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================
```

Gate	Instances	Area	Library
ADDFX1	263	5175.682	slow
AND2X1	25	113.535	slow
AND2XL	21	95.369	slow
AND3XL	2	12.110	slow
AND4X1	4	27.248	slow
AO21X1	2	13.624	slow
AO22X1	3	22.707	slow
AO22XL	34	257.346	slow
AOI211X1	10	52.983	slow
AOI211XL	13	68.878	slow
AOI21X1	96	435.974	slow
AOI21XL	238	1080.853	slow
AOI221X1	11	83.259	slow
AOI221XL	24	181.656	slow
AOI222XL	2	16.652	slow
AOI22X1	288	1743.898	slow
AOI22XL	728	4408.186	slow
AOI2BB1X1	11	66.607	slow
AOI2BB1XL	7	42.386	slow
AOI2BB2X1	1	9.083	slow
AOI2BB2XL	1	9.083	slow
AOI31XL	7	42.386	slow
AOI32XL	17	115.806	slow

AOI2BB2XL	1	9.083	slow
AOI31XL	7	42.386	slow
AOI32XL	17	115.806	slow
BUFX12	1	15.895	slow
BUFX16	1	21.193	slow
BUFX2	4	18.166	slow
BUFX20	1	25.735	slow
BUFX3	6	36.331	slow
BUFX6	21	190.739	slow
BUFX8	1	11.354	slow
CLKBUFX2	6	27.248	slow
CLKINVX1	454	1030.898	slow
CLKINVX12	8	96.883	slow
CLKINVX2	237	896.927	slow
CLKINVX20	1	19.679	slow
CLKINVX3	62	281.567	slow
CLKINVX4	2	12.110	slow
CLKINVX6	8	54.497	slow
CLKINVX8	3	27.248	slow
CLKXOR2X1	3	24.978	slow
DFFHQX1	163	2714.243	slow
DFFHQX4	4	87.800	slow
DFFHQX8	1	24.978	slow
DFFQX1	3391	53899.606	slow
DFFQX2	1	16.652	slow
DFFQX4	29	570.703	slow
DFFQXL	14	222.529	slow
INVX1	200	454.140	slow
INVX12	4	48.442	slow
INVX16	9	149.866	slow
INVX2	111	420.079	slow
INVX3	69	313.357	slow
INVX4	23	139.270	slow
INVX6	30	204.363	slow
INVX8	15	136.242	slow
INVXL	1418	3219.853	slow
INVX6	30	204.363	slow
INVX8	15	136.242	slow
INVXL	1418	3219.853	slow
MX2X1	157	1069.500	slow
MXI2X1	567	3862.461	slow
MXI2XL	276	1671.235	slow
NAND2BX1	28	127.159	slow
NAND2BX2	3	20.436	slow
NAND2BXL	7	31.790	slow
NAND2X1	134	507.123	slow
NAND2X2	6	36.331	slow
NAND2XL	4052	12267.835	slow
NAND3BX1	1	6.055	slow
NAND3BXL	6	36.331	slow
NAND3X1	25	113.535	slow
NAND3XL	11	49.955	slow
NAND4BX1	1	7.569	slow
NAND4BXL	2	13.624	slow
NAND4X1	23	139.270	slow
NAND4XL	46	243.722	slow
NOR2BX1	18	81.745	slow
NOR2BX2	5	34.060	slow
NOR2BXL	39	177.115	slow
NOR2X1	411	1555.429	slow
NOR2XL	891	2697.592	slow
NOR3BX1	6	36.331	slow
NOR3BXL	8	48.442	slow
NOR3X1	34	154.408	slow
NOR3XL	6	27.248	slow
NOR4BXL	1	6.812	slow
NOR4X1	1	6.055	slow
NOR4XL	3	18.166	slow
OA21X1	4	27.248	slow
OA21XL	22	149.866	slow
OA22X1	1	7.569	slow
OA22XL	93	703.917	slow

```
OAI211X1              6       31.790     slow
OAI211XL             25      132.458     slow
OAI21X1            2783    12638.716     slow
OAI21X2              16      133.214     slow
OAI21XL              84      381.478     slow
OAI221XL              1        7.569     slow
OAI222XL              2       16.652     slow
OAI22X1             439     2658.233     slow
OAI22XL             242     1465.358     slow
OAI2BB1X1           189     1001.379     slow
OAI2BB1X4             1       12.110     slow
OAI2BB1XL            25      132.458     slow
OAI32XL              15      102.181     slow
OR2X1               160      726.624     slow
OR2X2                26      137.756     slow
OR3XL                 2       12.110     slow
OR4XL                 2       13.624     slow
TBUFX4               15      193.010     slow
TBUFX6                1       23.464     slow
TLATNX1              16      230.098     slow
XNOR2X1               2       16.652     slow
XNOR2XL               2       16.652     slow
XOR2XL                1        8.326     slow
-----------------------------------------------
total             19052   125516.727


      Type       Instances     Area     Area %
-----------------------------------------------
sequential            3619   57766.608    46.0
inverter              2654    7505.420     6.0
buffer                  41     346.660     0.3
tristate                16     216.473     0.2
logic                12722   59681.565    47.5
physical_cells           0       0.000     0.0
-----------------------------------------------
total                19052 125516.727   100.0
```

Fig 37: 90nm Genus FD Gate count report

The Controller analysis using 90nm technology are depicted in below reports figures 38,39,40,41.

```
╞============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023   11:40:49 am
  Module:                 CONTROL_UNIT
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

   Instance     Module    Cell Count  Cell Area  Net Area   Total Area  Wireload
-------------------------------------------------------------------------------------
CONTROL_UNIT                   211   1706.053     0.000     1706.053    <none> (D)
  CTRL_I      CONTROLLER       103    927.959     0.000      927.959    <none> (D)
  PC_INST     PC                90    594.923     0.000      594.923    <none> (D)
  CTRLK_CLK_I CTRL_CLK          18    183.170     0.000      183.170    <none> (D)

 (D) = wireload is default in technology library
```

Fig 38: 90nm Genus Controller Area report

```
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023  11:40:49 am
  Module:                 CONTROL_UNIT
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

                    Leakage    Dynamic      Total
   Instance   Cells Power(nW)  Power(nW)   Power(nW)
--------------------------------------------------------
CONTROL_UNIT    211 10561.130 326627.5345 327683.6475
  CTRL_I        103  5549.679  11618.5161  12173.4840
  PC_INST        90  3641.517 166139.5535 166503.7051
  CTRLK_CLK_I    18  1369.934 124392.7639 124529.7573
  IR_I            0     0.000   7628.7019   7628.7019
```

Fig 39: 90nm Genus Controller total power report

```
  ====================================================================
    Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
    Generated on:           Nov 21 2023  11:40:49 am
    Module:                 CONTROL_UNIT
    Operating conditions:   slow (balanced_tree)
    Wireload mode:          enclosed
    Area mode:              timing library
  ====================================================================


  Path 1: VIOLATED (-618 ps) Setup Check with Pin CTRLK_CLK_I/CTR_reg[1]/CK->D
            Group: CLK100MHZ
       Startpoint: (R) CTRLK_CLK_I/CTR_reg[0]/CK
            Clock: (R) CLK100MHZ
         Endpoint: (R) CTRLK_CLK_I/CTR_reg[1]/D
            Clock: (R) CLK100MHZ

                      Capture       Launch
          Clock Edge:+     100            0
         Src Latency:+       0            0
         Net Latency:+       0 (I)        0 (I)
             Arrival:=     100            0

                Setup:-     136
          Uncertainty:-      10
       Required Time:=     -46
        Launch Clock:-       0
           Data Path:-     573
               Slack:=    -618
```

```
#-------------------------------------------------------------------------------------------------
#       Timing Point        Flags   Arc   Edge   Cell     Fanout Load Trans Delay Arrival Instance
#                                                            (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------
  CTRLK_CLK_I/CTR_reg[0]/CK -       -     R     (arrival)     14    -   100     -       0    (-,-)
  CTRLK_CLK_I/CTR_reg[0]/Q  -       CK->Q F     DFFQX4         3 14.9    55   372     372    (-,-)
  CTRLK_CLK_I/g2/Y          -       A->Y  R     XOR2XL         1  2.2    64   201     573    (-,-)
  CTRLK_CLK_I/CTR_reg[1]/D  <<<     -     R     DFFHQX4        1    -     -     0     573    (-,-)
#-------------------------------------------------------------------------------------------------
```

Fig 40: 90nm Genus Controller Timing report

```
|=============================================================
  Generated by:            Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:            Nov 21 2023  11:40:49 am
  Module:                  CONTROL_UNIT
  Technology library:      slow
  Operating conditions:    slow (balanced_tree)
  Wireload mode:           enclosed
  Area mode:               timing library
=============================================================
```

Gate	Instances	Area	Library
ADDFX1	4	78.718	slow
AND3XL	1	6.055	slow
AO22X1	5	37.845	slow
AOI211XL	1	5.298	slow
AOI21XL	13	59.038	slow
AOI22XL	2	12.110	slow
AOI32XL	1	6.812	slow
BUFX20	3	77.204	slow
CLKINVX1	7	15.895	slow
CLKINVX3	1	4.541	slow
CLKXOR2X1	1	8.326	slow
DFFHQX1	1	16.652	slow
DFFHQX2	7	121.861	slow
DFFHQX4	1	21.950	slow
DFFQX1	5	79.475	slow
DFFQX4	2	39.359	slow
INVX1	4	9.083	slow
INVX3	2	9.083	slow
INVXL	3	6.812	slow
MXI2X1	1	6.812	slow
NAND2BX1	2	9.083	slow
NAND2BXL	5	22.707	slow
NAND2X1	8	30.276	slow
NAND2X2	2	12.110	slow
NAND2XL	20	60.552	slow
NAND3XL	1	4.541	slow
NOR2BXL	4	18.166	slow
NOR2X4	2	19.679	slow
NOR2XL	31	93.856	slow
NOR3BXL	3	18.166	slow
NOR3XL	1	4.541	slow
NOR4X2	1	9.840	slow
OAI211XL	3	15.895	slow
OAI21X1	1	4.541	slow
OAI21XL	8	36.331	slow
OAI2BB1XL	2	10.597	slow
OAI31XL	1	6.055	slow
OR2X1	2	9.083	slow
SDFFQX4	1	24.978	slow
TLATNXL	20	287.622	slow
TLATX1	4	57.524	slow
TLATXL	21	302.003	slow
XNOR2X1	1	8.326	slow
XNOR2XL	1	8.326	slow
XOR2XL	1	8.326	slow
total	211	1706.053	

Type	Instances	Area	Area %
sequential	62	951.423	55.8
inverter	17	45.414	2.7
buffer	3	77.204	4.5
logic_abstract	1	0.000	0.0
logic	129	632.011	37.0
physical_cells	0	0.000	0.0
total	212	1706.053	100.0

Fig 41: 90nm Genus Controller gate count report

CONCLUSION:

The results in [9] has got the power value of 10.5mw, in [10] they got 1.72 mw power dissipation value, in [11], the authors mentioned the power value as 1.1649 mw. In [12], the authors got the power value as 17.85372661mw.The proposed work got the power report as 1.4789124211 mw for FD with no of cells as 19052 and 0.3276836475mw for controller with no of cells as 211, which are optimum results when compared with them[9,10,11,12].

FUTURE-SCOPE:

By integrating clock gating, power gating into the RISC processor design using Cadence tools, designers can achieve significant power savings during periods of inactivity, contributing to overall energy efficiency in embedded systems.

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BIBLIOGRAPHY

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