

# Simulation Of Optimized Low Power Cmos Digital Processor Design Using 32nm Technology

K Prasad Babu<sup>1</sup>, Dr. K.E. Sreenivasa Murthy<sup>2</sup>, Dr. M.N. Giri Prasad<sup>3</sup> 1Research Scholar (15PH0426), ECE dept, JNTUA, Ananthapuramu,

2Supervisor from JNTUA constituent college,

3Co-Supervisor from JNTUA College of Engineering,

Research Scholar, Jawaharlal Nehru Technological University Anantapur, Ananthapuramu

Associate Professor in ECE, Ashoka Women's Engineering College, Kurnool, Affiliated to Jawaharlal Nehru Technological University Anantapur, Ananthapuramu

Professor in ECE & Principal, Ravindra College of Engineering for Women, Kurnool, Affiliated to Jawaharlal Nehru Technological University Anantapur, Ananthapuramu

Adjunct Professor in ECE & Retired Director of Academics & Audit, JNTUA College of Engineering, Ananthapuramu, Constituent College of to Jawaharlal Nehru Technological University Anantapur, Ananthapuramu

ABSTRACT: In this work a CMOS based 4-bit processor is implemented with and without ANN. The foundry technologies used are 90nm, 45nm, 32nm. The simulations are performed and the power results along with no of MOSFETS are mentioned. The proposed work obtained promising results when compared with previous works. Nano processors utilize advanced fabrication techniques to create transistors and other components with nanoscale dimensions. These transistors can operate in conditions where classical physics laws may no longer directly apply and quantum effects can become significant. This introduces new challenges and opportunities for computing. In this research work, implementation of a 4-bit nano-processor utilizing Tanner Electronic Design Automation tool is proposed. The processor is developed using a cuttingedge 90nm, 45nm, 32nm technology files, focusing on achieving compactness, low power consumption, and efficient performance. The design process encompasses various stages, including schematic capture, simulation, and power analysis. The proposed Nano processor begins with a 4bit ALU that incorporates all fundamental and universal gates, an efficient and high-speed adder, multiplier, and multiplexer. The major subcomponents that can be changed are the Carry Save Adder and the multiplier. Power consumption and area reduction is optimised. The proposed Nano processor's second component is a 4-bit 6T SRAM, encoder and decoder, and an Artificial Neural Network. All of these subcomponents are created at the transistor level. Nano processors refer to a class of extremely small-scale integrated circuits designed to perform computation at the nanometre scale. The simulation results show for 90nm, power dissipation of 0.7009451 µW. For 45nm, power dissipation of 0.05211081µW. For 32nm, power dissipation of 0.0278810µW. With Power gating technique the obtained power is 0.05344917µw when compared with existing result. With Clock gating technique 6.044895 µW.

Keywords: Low Power, 4-bit Nano-Processor, 90nm, 45nm, 32nm, Power consumption, Power-Gating, Clock-Gating, ANN

# **INTRODUCTION**

The development of nano processors could lead to significant advancements in various fields such as discussed in below: 1. Miniaturization: Nano processors enable the creation of incredibly small computing devices that can be embedded in

everyday objects, leading to the proliferation of Internet of Things (IoT) devices and smart technologies. 2. High Performance: The smaller size of transistors in nano processors can potentially lead to faster and more energyefficient computations, pushing the boundaries of computational power.

3. Quantum Computing: At the extreme nanoscale, quantum effects become prominent. Quantum processors exploit these effects to perform certain types of computations that are exponentially faster than classical computers for specific problems.

4. Biomedical Applications: Nano processors can be used in medical devices, drug delivery systems, and even inside the human body for various diagnostic and therapeutic purposes.

5. Energy Efficiency: As transistors become smaller, they typically consume less power, potentially leading to more energyefficient computing systems.

However, developing and manufacturing nano processors comes with numerous challenges, including managing heat dissipation, dealing with quantum effects, and designing reliable components at such a small scale.4-bit Nano-Processor in this term "4-bit" suggests that the processor deals with data in 4-bit values. In computing, the number of bits in a processor's

data path influences its capabilities and limitations. A 4-bit processor would typically handle relatively simple tasks due to its limited data width. Low Area, Low Power, and Minimum Delay These are the key goals of the design. "Low area" refers to the desire for the processor's physical size to be minimized. "Low power" signifies an emphasis on energy efficiency, aiming to reduce the amount of power the processor consumes. "Minimum delay" implies a focus on optimizing the speed of the processor's operations. The study would involve both the theoretical design of the processor's architecture and the practical implementation using the specified technology. The subsequent performance analysis would assess how well the processor meets its design goals and may involve simulations, measurements, and comparisons with other processor designs. The design focuses on achieving low physical size, minimal power consumption, and fast operation. This includes optimizing the processor's architecture for these goals. The performance analysis assesses how well the design meets these objectives by measuring its area usage, power efficiency, and operational delay. The research paper aims to demonstrate the feasibility of a highly efficient and compact 4-bit processor using CMOS technology. The power in CMOS circuits is dynamic & static power dissipation. The dynamic power equation is given by  $P_{dyn}=1/2 \ C \cdot V^2 \cdot f$ , where C is the total capacitance that is being switched per clock cycle.V is supply voltage, f is the clock frequency. The Leakage power is given by  $P_{leak}= I_{leak}$  V, where  $I_{leak}$  is the leakage current. V is supply voltage.

# **LITERATURE SURVEY:**

Many authors contributed much of their focus on low power design of digital processor, a few of the represented here. In [1], the authors proposed 4-bit nano processor with FINFET technology, with power dissipations of 2.68µw (without ANN) and 1.98µw (with ANN), overall design was 314.4µW for 32-nm. In[2], authors mentioned about using the combination of CG & PG for 4-bit digital processor with power dissipation of 0.147mw (45nm), 2.375mw(90nm). In [3], authors mentioned about usage of CG for 4-bit digital Processor with the value of 233µw (45nm). In [4], authors have represented the design of power gated ALU, with power as 2.15 µw. In[5], the authors have discussed about the low power digital design survey. In [6], the authors contributed about the 1-bit finfet FA cells using 16nm. In [7], the authors have elaborated about the Finfets & its architectures. In [8], authors have presented optimization ALU with power gating technique. In [9], authors have contributed on dynamic circuit technique for low power processor design. In [10], author represented about the design & fabrication of 4-bit processor. In [11], authors evaluated the performance of 4-bit ALU with power value of 1.759 mw. In [12], the authors worked for power consumption of embedded processors & proposed 3 operating modes High-Performance mode, Normal mode, Low-power mode. The average amounts of power consumed by the respective modes are 41.7 µW, 59.7 µW and 71.1 μW. In[13], 5.9414mw. In[14], the authors has represented a stable 4-bit arithmetic logic unit (ALU) design using a minimum number of transistors that can overcome the limitations of printed devices. In [15], the authors proposed the 4-Bit ALU designed using the full-swing GDI technique, with power dissipation as 0.1541nw as average power. In [16], the authors represented the study and analysis of various contributions towards low power processor design techniques.

### **Proposed Design:**

This section deals with the proposed 4bit nano processor design methodology & block representation. The proposed design differs from existing approach<sup>1</sup> with the usage of CMOS gates instead of FinFet, Usage of basic gates and optimised gates. The entire work is distributed as Basic design with CMOS gates, without ANN, CG, PG & with optimised CMOS gates, with ANN, CG & PG. The results are simulated using 90nm technology file, 45nm technology library file and 32nm library file. The important blocks in the design are 4-bit ALU which is composed of mux based. The SRAM circuitry is simulated single bit & 4-bit with and without CG,PG. In the work of the author<sup>11</sup> both analog & digital ALU were implemented and the power dissipated values were 1759µw, 5.360 µw respectively. In [13], the authors got the power value as 23.93mw with FInFET transistors. All the designs are operated with a supply voltage of 0.07 - 1.2v. In the existing method<sup>1</sup> the author used fingering concept, which engage in improvement the resistance of the gate poly terminal along the width of the transistor. With this technique the area and capacitance can be enhanced. Dynamic Power Consumption is associated with the charging and discharging of capacitors during switching. Primarily occurs during active operation when the circuit is actively processing data or executing instructions and directly related to the frequency of clock signals and the rate of switching. Static Power Consumption happens from leakage currents in transistors even when they are not actively switching. It is present during both active and idle states, contributing to power consumption even when the circuit is not performing computations and becomes more significant in advanced semiconductor technologies with smaller feature sizes and lower threshold voltages.

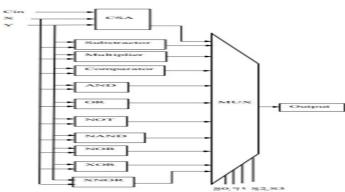


Fig A: Architecture of 4bit ALU with Input-combination of 11 MUX

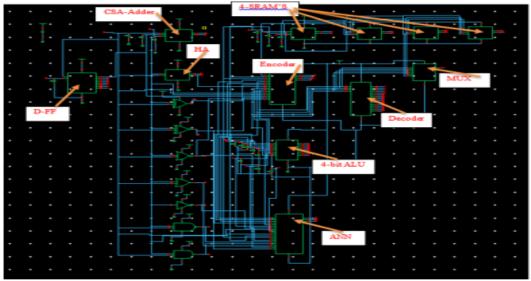


Fig B - Schematic of Existing 4 bit nano processor design

Figure B depicts about the existing system design of the design.

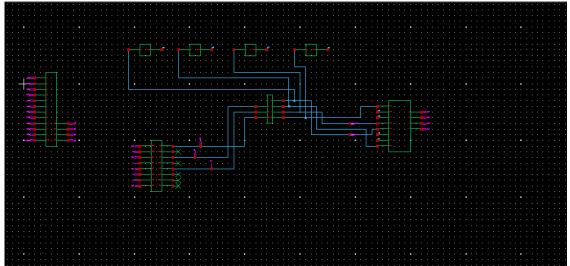
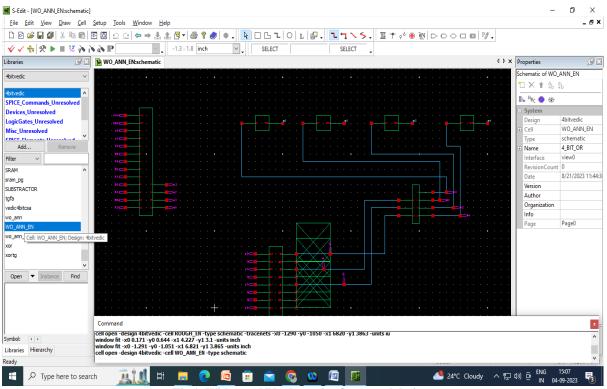


Fig C - Schematic of Proposed 4 bit nano processor design

To simplify the architecture, the processor is represented with the basic ALU, Encoder Decoder & ANN block as shown in figure C.

### Simulation Results:

All the results are simulated using tanner EDA tool. The technology library files used are 90nm, 45nm, 32nm.





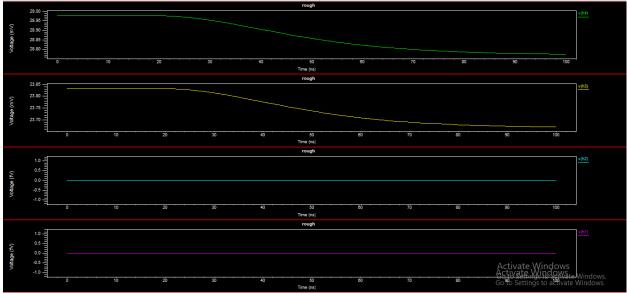


Fig 2: Waveform for Proposed 4 bit nano processor design

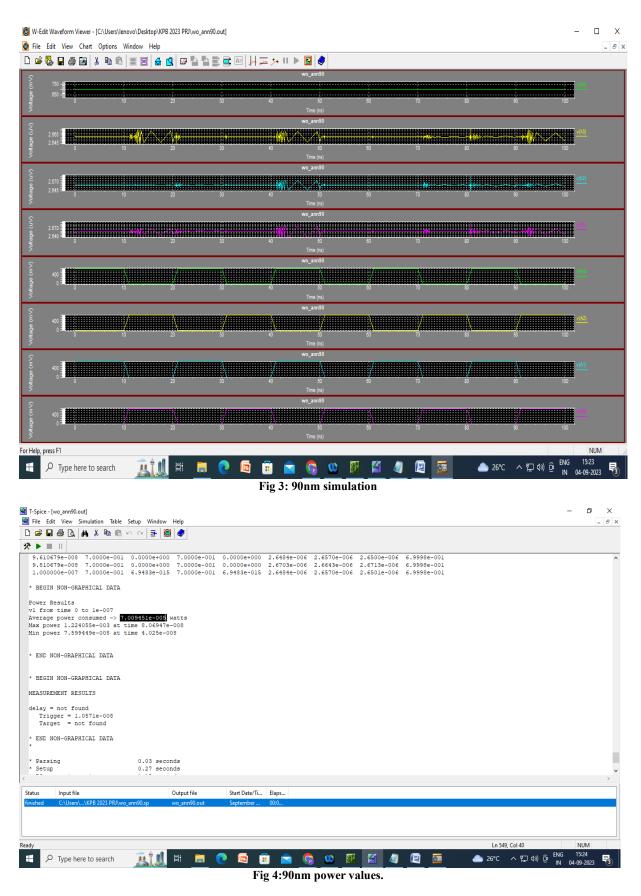


Fig 4 shows the power value of 1.224mw maximum and average power of 0.1224µW using 90nm technology.

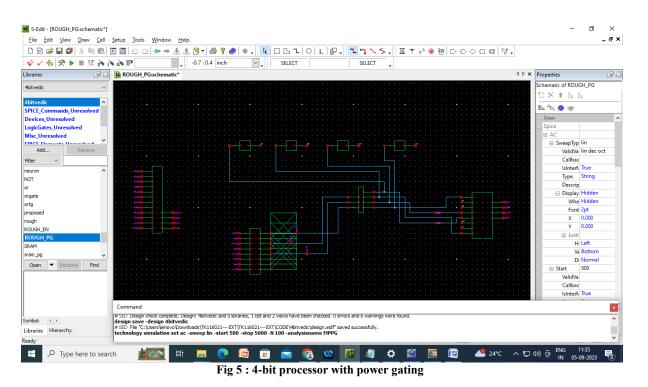


Fig 5 indicates the PG technique employed for power reduction of the proposed design.

		Options Window			11							-
<u>نه</u>		x • 6 = 8	🗟 😫   🖾 🖺		₩ ឝ ៚ ॥	ROUGH PG						_
	1.0 0.0 <b>=</b>											
	-1.0	10	20	30	40	50 Time (ns) ROUGH_PG	60	70	80	90	100	
	-1.0	10	20	30	40	50 Time (ns) ROUGH PG	60	70	80	90	100	
	1.0										v(n2)	
	0.0 -1.0 0	10	20	30	40	50 Time (ns)	eo	70	80	90	100	
	1.0					ROUGH_PG						
	-1.0	10	20	30	40	50 Time (ns)	80	70	80	90	100	
						ROUGH_PG						
	400	10	20	30	40	50 Time (ns)		70	80	90	100	
						ROUGH_PG						
	400	10	20	30	40	50 Time (ns)	60	70	80	90	100 v(A2)	
						ROUGH_PG						-
	400	10	20	30	40	50 Time (ns)	80	70	80		100 v(A1)	
						ROUGH_PG						
	400	10	20	30	40	50 Time (ns)	80	70	80	90	100	
lp, pr	ess F1										NUM	4
	P Type here to	search 🕌		- 🔊 🕞	3 💼 🗲	00 🔊 🕯	<b>R</b>	🌣 🌌 🗟	= 🤷	24℃ ヘロが	) 📴 ENG 11:34 IN 05-09-2023	

Fig 6: simulation of power gating

) 🗳 日	i 🗇 📐 👧 👗 🖻 💼	က က 📑 🔯	0									
•		1-1-										
9.0250	00e-008 1.7500e-001	5.2500e-001	1.7500e-001	5.2500e-001	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000				
	85e-008 6.2500e-001			7.5000e-002			0.0000e+000	0.0000e+000				
	000e-008 7.0000e-001							0.0000e+000				
	14e-008 7.0000e-001			0.0000e+000			0.0000e+000	0.0000e+000				
	14e-008 7.0000e-001		7.0000e-001		0.0000e+000		0.0000e+000	0.0000e+000				
	14e-008 7.0000e-001						0.0000e+000	0.0000e+000				
	14e-008 7.0000e-001			0.0000e+000 0.0000e+000				0.0000e+000 0.0000e+000				
	000e-007 7.0000e-001							0.0000e+000				
BEGIN	NON-GRAPHICAL DATA											
	lesults time 0 to le-007											
verage	power consumed $\rightarrow 4$ .											
	power consumed -> 4. ver 4.900000e-013 at t		vacca									
lax pow	ver 4.900000e-013 at t	cime O	12005									
lax pow		cime O	acts									
ax powe	ver 4.900000e-013 at t	cime O	acca									
END N	ver 4.900000e-013 at t ver 4.900000e-013 at t	cime O										
END NO BEGIN	ver 4.900000e-013 at t ver 4.900000e-013 at t NON-GRAPHICAL DATA	cime O										
END NO BEGIN EASURE	ver 4.900000e-013 at t ver 4.900000e-013 at t NON-GRAPHICAL DATA NON-GRAPHICAL DATA MENT RESULTS	cime O										
END NO BEGIN EASURE elay =	ver 4.900000e-013 at t ver 4.900000e-013 at t NON-GRAPHICAL DATA NON-GRAPHICAL DATA MENT RESULTS • not found	cime O										
END NO BEGIN CASURE 21ay = Trigo	ver 4.900000e-013 at ver 4.900000e-013 at NON-GRAPHICAL DATA NON-GRAPHICAL DATA MENT RESULTS - not found ger = 1.0571e-008	cime O										
END NO BEGIN CASURE 21ay = Trigo	ver 4.900000e-013 at t ver 4.900000e-013 at t NON-GRAPHICAL DATA NON-GRAPHICAL DATA MENT RESULTS • not found	cime O										
END NO BEGIN EASURE EASURE Trigg Targe	ver 4.900000e-013 at ; ver 4.900000e-013 at ; NON-GRAPHICAL DATA i NON-GRAPHICAL DATA i NON-GRAPHICAL DATA i NON-GRAPHICAL DATA i NON-GRAPHICAL DATA ger = 1.0571e-008 jet = not found	ime 0		Start Data/Tc	Flore							
ax power in power END NO BEGIN EASUREN elay = Trigg Targe	ver 4.900000e-013 at t ver 4.900000e-013 at t NON-GRAPHICAL DATA D NON-GRAPHICAL DATA MENT RESULTS * not found rger = 1.0571e-008 ret = not found Inputfile	ime 0	Output file	Start Date/Ti	Elaps							
END No BEGIN EASUREN elay = Trigg Targg tus	<pre>ver 4.900000e-013 at ; ver 4.900000e-013 at ; NON-GRAPHICAL DATA NON-GRAPHICAL DATA NENT RESULTS = not found ger = 1.0571e-008 get = not found Input file C.NUseryLocal.Temp\ROL</pre>	ime O	Output file ROUGH_PG.out	September	00:0							
END N END N BEGIN CASURE CASURE Trigg Targe	ver 4.900000e-013 at t ver 4.900000e-013 at t NON-GRAPHICAL DATA D NON-GRAPHICAL DATA MENT RESULTS * not found rger = 1.0571e-008 ret = not found Inputfile	ime O	Output file									
END No BEGIN EASUREN elay = Trigg Targg tus	<pre>ver 4.900000e-013 at ; ver 4.900000e-013 at ; NON-GRAPHICAL DATA NON-GRAPHICAL DATA NENT RESULTS = not found ger = 1.0571e-008 get = not found Input file C.NUseryLocal.Temp\ROL</pre>	ime O	Output file ROUGH_PG.out	September	00:0							
ax power in power END NO BEGIN EASUREN elay = Trigo Targo	<pre>ver 4.900000e-013 at ; ver 4.900000e-013 at ; NON-GRAPHICAL DATA NON-GRAPHICAL DATA NENT RESULTS = not found ger = 1.0571e-008 get = not found Input file C.NUseryLocal.Temp\ROL</pre>	ime O	Output file ROUGH_PG.out	September	00:0				Ln 16	59, Col 34	NUM ENG 11:36	

In the figure 7 the max power obtained is 49000 nw which is very less when compared with the existing system design of  $314.4 \ \mu w$ 

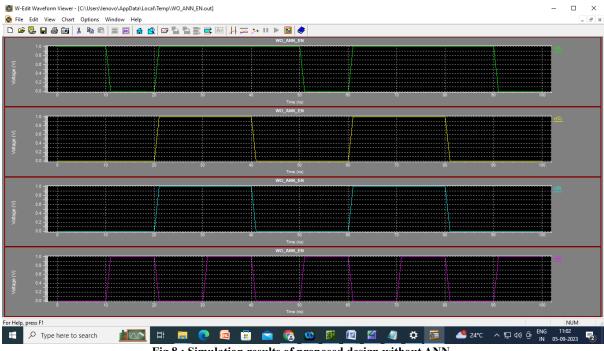


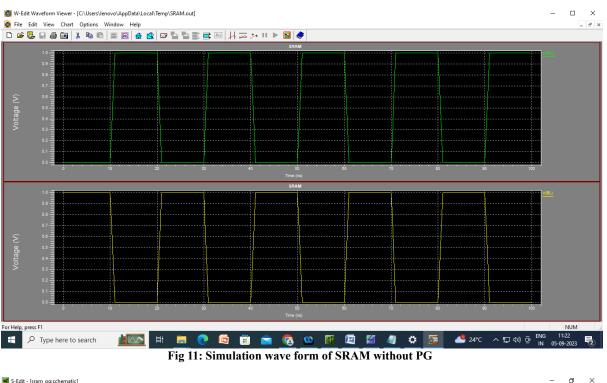
Fig 8 : Simulation results of proposed design without ANN

<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>D</u> raw <u>C</u> el	Setup Tools Window Help		- 8
) 🖻 📽 🖬 🕼 🕺 X 🖻 🖻			
🗸 🗸 🔩 🛠 🕨 🗉 👯 🏹	N & IP 1.7:2.8 inch SELECT		
raries 😥	🛛 📔 SRAMschematic 4 🗅 🗙	Properties	Ø
itvedic		Schematic of SRA	M
	•••••••••••••••••••••••••••••••••••••••	10 × 🕯 🚯	åb
tvedic 🖌		🛼 Asr 🥏 😻	
ICE_Commands_Unresolved			
vices_Unresolved		<ul> <li>System</li> <li>Design</li> </ul>	4bitvedic
gicGates_Unresolved		E Cell	SRAM
sc_Unresolved	• • • • • • • • • • • • • • • • • • • •	Туре	schematic
Add Remove		Name	4 BIT OR
er 🗸		Interface	view0
iron /		RevisionCount	5
r.		Date	8/9/2023 12:3
		Version	
ate		Author	
,		Organization	
posed		Info	
gh		Page	Page0
JGH_EN			
UGH_PG			
АМ			
m_pg			
Open 🔻 Instance Find			
BL QB			
	Command		
	window ft -x0 -5,21 -y0 -5,631 -x1 14,804 -y1 6,493 -units inch		_
bol: + + 4_BIT_OR of 1	window fit -x0 -0.694 -y0 -0.775 -x1 9.315 -y1 5.287 -units inch		·
raries Hierarchy	window fit -x0 -6.09 -y0 -3.813 -x1 13.928 -y1 8.315 -units inch cell open - design Abitvedia -cell SRAM -type schematic		
ły			
	arch 🔢 💽 🗮 📻 💽 👼 💼 🕋 🚱 🥨 🕎 👰 🌠 🥒 🔅 💶 24°C 🗛 🖫 4	- ENG	11:19 -09-2023

The SRAM internal schematic of the basic SRAM circuit is presented in figure 9.

T-Spice - [SRAM.out] File Edit View Simulation Tab	ole Setup Window Help				- 0
i 🛎 🖬 🍜 🖪 🗛 🕺 🖻 i	🛍 느 ㅋ   포   🔯   🥏				
E ▶    II					
9.925000e-008 0.0000e+0 1.000000e-007 9.9262e-0					
* BEGIN NON-GRAPHICAL DAT	Ά.				
Power Results v1 from time 0 to 1e-007 Average power consumed -> Max power 1.440000e-012 a	at time 0				
Min power 1.440000e-012 a	t time 0.				
* END NON-GRAPHICAL DATA *					
* Parsing	0.00 seconds				
* Setup * DC operating point	0.01 seconds 0.00 seconds				
* Transient Analysis	0.00 seconds				
* Overhead *	1.03 seconds				
* Total	1.04 seconds				
* Simulation completed w	vith 5 Warnings				
* End of T-Spice output f	tile.				
ind of 1 opide dadpad 1					
atus Input file	Output file	Start Date/Ti Elaps			
nished C:\Users\\AppData\Loo	cal\Temp\sram_pg.sp sram_pg.out	September 00:0			
nished C:\Users\\AppData\Loo		September 00:0			
nished C:\Users\\AppData\Loo		September 00:0 September 00:0			
nished C\Users\\AnnData\Lo	tar ( temp ( sta innsp ) sta innout				
nished C:\Users\\AppData\Loo					
nished C:\Users\\AppData\Loo				Ln 152, Col 40	NUM
	i 🔜	0 🖬 🛱 🐋 🕫	) 🗱 🔄 🌠 🍕		

Basic SRAM circuit without PG is dissipating a value of 1.44 pw as shown in figure 10.



<u>File Edit View Draw Cell</u>	Setup	Tools	Window	w <u>H</u> elp	р																	- 5
D 🖻 🚅 🖬 🕼 👗 🖻 💼	A 10	00			t. 🖪 🕶	8 ?		- <b></b>	06-	LOI	.   ₽	. 1	<b></b>	5.	區 <b>十</b> (	çð 🔘 i	èn   🕞		PØ -			
🗸 🗸 🐁 🛠 🕨 🔳 🐯 🔊	1 øg ø	P		~ <u>.</u>	4.7 : 2.	3 inch			SELECT	1	NOVE	-	SELECT	- 1								
oraries 🖉 🗵	🖬 sra	m_pg:so	chematic																4 Þ	×	roperties	ø
oitvedic v							•								•				•	S	hematic of srar	n_pg
																				1	5 🗙 🕇 🛼	åb
itvedic ^																					🔈 Age 🔗 😸	
ICE_Commands_Unresolved																					System	
vices_Unresolved																					Design	4bitvedic
gicGates_Unresolved	•																				Cell	sram_pg
isc_Unresolved																					Туре	schematic
Add Remove																					Name	4_BIT_OR
er v											$\ge$										Interface	view0
																					RevisionCoun	at 0
iron ^										× i											Date	8/21/2023 2:
т																					Version	
							•			•			•								Author	
ate																					Organization	
9												$\sim$			$\square$						Info	
posed	Ľ.								Ľ	<u> </u>		$\square$			1X						Page	Page0
igh UGH EN								<u>×</u> —	$-\times$					$\boxtimes$	4					11	-	
UGH PG	•								· • 1	1	•	•		<u> </u>	A							
AM									N 2						×							
m_pg v							+			Ļļ _	. L	ЩĻ,										
									L		$\times$	L										
Open 🔻 Instance Find																						
	•																					
w_ q																						
BL QE	6	mand																				
bol: + + 4_BIT_OR of 1			theck comp 0 -5.21 -y						2 views hav	/e been che	cked. 0 e	errors and	35 warn	ings were	found.							
raries Hierarchy	windo	w fit -x	0 -0.694	-y0 -0.7	75 -x1 9	315 -y1	5.287 -u	nits inch														
dy	windo	W TIE -XO	0 -6.09 -1	70 -3.81	5 -XI 13.	.928 -y1	o.315 -U	mus inch														
			_			-	-	-		-	_		-					 			ENG	11:09
P Type here to searchere	rch		$\sim$							5	00	新				D.	0	😃 24°C	: ^ १	口 (s))	Gi ENG	5-09-2023

### Fig 12 : SRAM schematic with PG

	dit View Chart Options		n		<u>∼</u> •• II b							
× 42						sram_pg						l vivila
	0.9											
	0.8											
	0.8											
	0.4											
	0.3											
	0.1											
		10	20	ao '	40 · ·	50 Time (ns)	·	70	ʻ soʻ	· · · 90	100	•
	1.0					sram_pg				- in		<u>v(BL)</u>
	0.9											
	0.7											
	0.5											
	0.4											
	0.2											
	0.0	10	20	30	40		80	70	80		100	
						Time (ns)						NUM
	SS F1 7 Type here to search		Hi 🔒	2	-		-	<u>ଣ 🧠 ଅ</u>		<u>∕</u> ¶ 24°C	ヘロの値	NG 11:08 N 05-09-2023
ice -	[sram_pg.out]					ulation of	f PG-SRA					- 0
oice - e Ec ≩ ∎	[sram_pg.out] lit View Simulation Tabl											
oice - ₽ Ec ₽ E	[sram_pg.out] fit View Simulation Tabl G C A A S C C II II II 00000−008 0.00000+00	]ທດ  <u>₹</u>  ] 0 1.0000e+00	v Help									- 0
oice - E Ec 925	[sram_pg.out] ift View Simulation Tabl	0 1.0000e+00 5 1.0000e+00	v Help									- 0
ice - Ec 925 000 EGII	[sram_pg.out] iit View Simulation Tabl iii II 0000-001 A A A A A 0000-001 S.2222-01 N NON-GRAPHICAL DATA Results	0 1.0000e+00 5 1.0000e+00	v Help									- 0
ice - EC 925 0000 EGII from rag.	[sram_pg.out] iit View Simulation Tabl iii Dia A A A A A A 1000e-008 0.0000e+00 000e-007 9.9262e-01 N NON-GRAPHICAL DATA	1.00000e=012 time 0	v Help									- 0
bice - e Ec 9250 0000 BEGII from trage	[sram_pg_out] dit View Simulation Tabl dit View Simulation Tabl dit View Simulation Tabl dit View Simulation Table 0000-0008 0.00000+00 0000-0008 0.00000+00 0000-0007 9.5262e-01 N NON-GRAPHICAL DATR Results m time 0 to 1e-007 e power consumed -> uer 1.000000e-012 at	1.00000e=012 time 0	v Help									- 0
er l polo er l from rage polo ND l ars. etu	<pre>(sram_pg.out) it View Simulation Tabl it View Simulation Tabl it 0000e-0008 0.00000e+000 000e-0007 9.9262e-01 N NON-GRAPHICAL DATA Results m time 0 to le=007 wer 1.000000e-012 at wer 1.000000e-012 at NON-GRAPHICAL DATA ing p</pre>	0 1.0000e+00 5 1.0000e+00 1.00000e-012 time 0 time 0 0.01 sec 0.00 sec	v Help v Help									- 0
sice - E Ec 9255 0000 EGII rago rago ND 1 ars. etu C op	[sram_pp_out] iit View Simulation Table iit Oice Construction Table iii Oice Construction Table 0000-000 A state of the Construction 0000-000 S.2262e-01 N NON-GRAPHICAL DATA NON-GRAPHICAL DATA ing perating point sient Analysis	0 1.00000e-012 1.00000e-012 time 0 0.01 sec 0.00 sec 0.00 sec 0.00 sec 0.00 sec	v Help C C C C C C C C C C C C C C C C C C C									- 0
er l e Ed e Ed er l from rage	[sram_pp_out] iit View Simulation Table 0000-005 0.00000e+00 00000-007 9.9262e-01 N NON-GRAPHICAL DATA Results m time 0 to le-007 power 0.000000e-012 at NON-GRAPHICAL DATA ing perating point sient Analysis head	0.01 sec 0.00 sec 0.00 sec	v Help v Help									- 0
Pice - ce Ec P 250 0000 BEGII from a por a por crage crag	[sram_pp_out] iit View Simulation Table 0000-005 0.00000e+00 00000-007 9.9262e-01 N NON-GRAPHICAL DATA Results m time 0 to le-007 power 0.000000e-012 at NON-GRAPHICAL DATA ing perating point sient Analysis head	0 1.0000e+00 5 1.0000e+00 5 1.0000e+00 5 1.0000e-012 time 0 time 0 time 0 0.01 sec 0.00 sec 0.00 sec 0.00 sec 1.03 sec	v Help 0 0 0 0 0 0 0 0 0 0 0 0 0									- 0
ice E Ec 9255 0000 EGII EGII EGII ND 1 Ars. Setu Verl Cotal Simu	[sram_pg_out] ii: View Simulation Table ii: View Simulation Table ii: View Simulation Table ii: View Simulation Table view Construction Construction NON-GRAPHICAL DATA NON-GRAPHICAL DATA ing perating point sient Analysis head	0 1.0000e+00 5 1.0000e+00 5 1.0000e+00 time 0 time 0 time 0 0.01 sec 0.00 sec 0.00 sec 0.00 sec 1.03 sec 1.04 sec	v Help 0 0 0 0 0 0 0 0 0 0 0 0 0									- 0
ice EGII er 1 froi por ND 1 ars. etun Con veri 	[sram_pg_out] if: View Simulation Table iii View Simulation Table iii A A A A A A A A A A A A A A A A A A	0 1.0000e+00 5 1.0000e+00 5 1.0000e+00 time 0 time 0 time 0 0.01 sec 0.00 sec 0.00 sec 0.00 sec 1.03 sec 1.04 sec	v Help 0 0 0 0 0 0 0 0 0 0 0 0 0									- 0
sice	<pre>[sram_pg_out] it View Simulation Tabl div View Simulation Tabl div D</pre>	0 1.0000e+00 5 1.0000e+00 5 1.0000e+00 time 0 time 0 time 0 0.01 sec 0.00 sec 0.00 sec 0.00 sec 1.03 sec 1.04 sec	v Help 00 00 2 watts 2 watts 2 watts 2 matts 2 mat	Fig	13: Sim							- 0
eed	[sram_pg.out] II: View Simulation Table II: View Simulation Table II: View Simulation Table II: View Simulation Table II: View Simulation NOODE-0007 9.9262e-01 N NON-GRAPHICAL DATA Results m time 0 to 1e-007 e power consumed -> wer 1.000000e-012 at NON-GRAPHICAL DATA ing perating point sient Analysis head 1 lation completed wi of T-Spice output fi Inputfile ClUbers/local/TemplW	0 1.000000-012 1.000000-012 time 0 time 0 0.01 sec 0.00 sec 0.00 sec 0.00 sec 1.04 sec th 5 Warning 1e	v Help 00 00 00 00 00 00 00 00 00 0	Fig 1	13: Sim							- 0
sice - Ec 9250000 EGII errig por por errag por errag por errag rag rag ind ind ind ind ind	[sram_pg_out] iit View Simulation Tabl iit Oice Simulation Tabl iii Oice-007 8.0.00000+00 0000-008 0.000000+01 9.5262e-01 N NON-GRAPHICAL DATA ing proper consumed -> wer 1.000000e-012 at NON-GRAPHICAL DATA ing proper consumed -> ing pr	0 1.000000-012 1.000000-012 time 0 time 0 0.01 sec 0.00 sec 0.00 sec 0.00 sec 1.04 sec th 5 Warning 1e	v Help 00 00 00 00 00 00 00 00 00 0	Fig 1	13: Sim							- 0
pice - e Ec 2 225 2 2000 3 EGII from 2 2000 5 2000	[sram_pg.out] II: View Simulation Table II: View Simulation Table II: View Simulation Table II: View Simulation Table II: View Simulation NOODE-0007 9.9262e-01 N NON-GRAPHICAL DATA Results m time 0 to 1e-007 e power consumed -> wer 1.000000e-012 at NON-GRAPHICAL DATA ing perating point sient Analysis head 1 lation completed wi of T-Spice output fi Inputfile ClUbers/local/TemplW	0 1.000000-012 1.000000-012 time 0 time 0 0.01 sec 0.00 sec 0.00 sec 0.00 sec 1.04 sec th 5 Warning 1e	v Help 00 00 00 00 00 00 00 00 00 0	Fig 1	13: Sim					Ln 154,	Col 34	- 0

The power dissipation obtained is 1 pw with PG of SRAM circuit. There is a variation of 30 % in power dissipation.

	dit <u>V</u> iew	<u>D</u> raw			Tools	Windov	<u>H</u> el	р																			- 8
Ľ 🖻	🛩 🖬 🕼	X 🗈	i 🔁 🔁	- <b>X</b> X	<u>n</u> 2	$\Leftrightarrow \Rightarrow$	1	L 🖪 🕶	1 🗇 💡	🥏   🖷 .	- R		20	) L	d -	1 7 7	- 5 -	正 🕇	· 👌 🖲	<u>≹</u> N   ⊡	- $ -$		P/ -				
44	🛧 🖈 🕨	. <b>1</b> .	10	a`s IP	•		~	9.2 : 3	.3 inch		∽	SELE	ст			SELECT											
braries		9 🛛	12_AN	D:sche	matic																			4 Þ 🗙	Properties	s	g
oitvedic		~	•	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	Schematic	of 2_At	ND.
JACT COIC																									$\infty \times \infty$	1 26 3	2b
oitvedic		^																							B. PBc (		
																									Syster		
_Pads					1.				<u>t</u>	ha to a				·						Aut					Design		4bitvedic
gicGates PICE_Ele				i:	1000	g E ins		- E		e in			= <u>1</u> 12		= 111				a	Ed = int	1				TE Cell		2 AND
ICE_EIE	merns		1			T					G E ken										AT E lan				Type		schematic
Add	Remo	ve				rdE	102														1			· ·	Name		4_BIT_OR
ter	~			-	N = im	-1 t			ad i	# -~	2 - ±12			n in the second s					and in	-	tā ≣ ģip				Interfa	ce	view0
AND		^			<b>b</b> -}		- Alla -		• d		<b>1</b> -1			<b>1</b>					10 I I					•		onCount	
NAND														2 C 1 4											Date		8/5/2023 4:09:
NOR					e in the second				-	•				<b>1</b>					- (e)					•	Version		
OR					<u> </u>																				Autho		
XNOR																									Organi	ization	
XOR																											Page0
it																									Page		Fageo
ittg																								Ľ.			
ND																											
NDtg r																								•			
pen 🔻	nstance F	ind																						•			
	<b></b>																										
	< > 4_BI	T_OR ¢		mmand																							×
oraries	Hierarchy		wine	low fit	-x0 7.69	7 -y0 0.	998 -x	1 13.044	-v1 4.08	3 -units in 9 -units ir	nch																^
idy			wine	low fit	-x0 5.08	36 -y0 -1	.07 -x	15.78	y1 5.116	-units inc	h .																0

Fig 15: Schematic of 4-bit basic AND

The basic cmos 4-bit AND-gate is revealed in fig 15.

ו 🛋 🖻 נ	🖬 💷 🐰	Pob (63)	15 K	1 2 4	⊇  ቀ=	→ .±.	1. 🖪	-   🕾	ን 😵 🦪		- <u>F</u>	- C. T	- 0 1	ь   🗗 🗸		1 🔨 ≶	• III -	🕈 🕫 🍕	▶ <u>₹</u> N   c	> 0 0		PØ 🗸			
/ 🗸 🚓	** 🕨 🔳	😻 🔖 i	× a>	IP		$\sim$	-0.	1:1.3	inch		~ <b>.</b>	SELECT			SE	LECT									
raries	<i>9</i> 🛙	🖬 2_	NAND	schema	tic																		4 Þ 🗙	Properties	9
tvedic	~																							Schematic of 2_N/	
																								10 × ± %	9b
tvedic	^	•																						18 PBc 😐 😻	
Pads																								<ul> <li>System</li> </ul>	
jradis jicGates																								Design	4bityedic
CE_Element																								(# Cell	2_NAND
CC_Dement																								Type	schematic
Add	Remove	•																						+ Name	4_BIT_OR
r v		1									-													Interface	view0
ND					. –																			RevisionCount	1
AND				60 m m						:		12		- Bin	1000 J	- <b>1</b> 8 - 144				a i in	الم محمد	E 100		Date	8/5/2023 4:0
DR					e1 (2																			Version	
R											· · ·										•			Author	
NOR																								Organization	
OR											1 = 1m				and the line					194900.00	and E is the second			Info	
					- E1	- 22					1				leg -						ller j			Page	Page0
to																									
ND OIL											1 200				in a second second										
NDtg											11.										11 · · ·				
	~																								
en 🔻 nst	tance Find																								
ool: 4	4_BIT_OR		Commi	bod																					×
	erarchy	2 I I I I I I I I I I I I I I I I I I I	indow	nt - xu 7	.697 -VI	J U.99N	-81 1.1.	044 - 11	4.089 -	unitsi	nch														
aries Plie	erarcity		indow	fit -x0 5	.086 -y	0-1.07	-x1 15.7	78 - v1 5	5.116 -u y1 7.16	nits inc	ah in														^

Figure 16: schematic of basic NAND

The necessary cmos 4-bit NAND-gate is illustrated in fig 16.

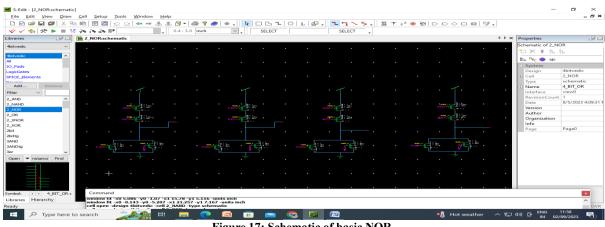
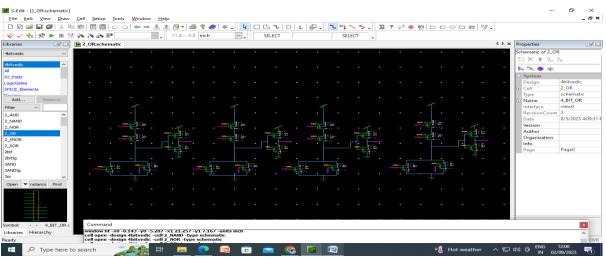
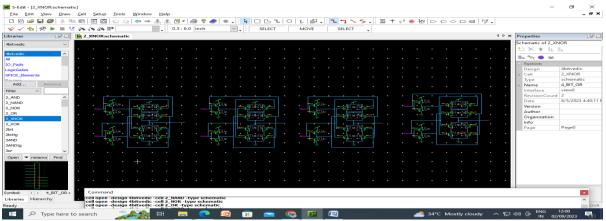


Figure 17: Schematic of basic NOR

The fundamental cmos 4-bit NOR-gate is described in fig 17.









Eile Eo	it ⊻iew	Draw	<u>Cell S</u> eti			indow	Help		6			11			- 1.		1.0	1		-			ç* 🖷					. 1					- 8
	- 641 64P	35 ULA	v> i> a				***	· 🐨 👻	3.6 inc	? 🥏		- -		] [] SELEC			ra <mark>₽</mark>	-	SELECT		- 10	<i>к</i> . т.	¢ <sup>0</sup> 🥶	9 QIN			0		-				
braries	a x. 🛌	e ei	₩ 2_XOR:			_	-	0.010	s.o jine		-	- I	<u>.</u>	SELEC				_	SELECT		-								4 6	-	Properties		G
			Z_XOR	schema	ю																								4.6		Properties Schematic of 2_	KOR	5.99
vitvedic		~																													to × ± s		
itvedic		^																															
																															🛼 🔤 🔿 🗟	Je .	
Pads																														6	System		
gicGates																															Design	4bitvedi	c
ICE_Elen	ents																													1 9	Cell	2_XOR schema	
Add	Remo	Ve																													Type Name	4_BIT_O	
ter	V	~~																													Interface	view0	R.
	~	0																													RevisionCou		
AND NAND		^		۲.		• •	Ŀ.			1							4			,			5			1	٦.				Date	8/5/202	3 4:09
NOR				THE R. L. L.		dillor to	6. mar 1			THE .			Local and	-		. tr	age days		au autor							in the r	<u>.</u>				Version		
OR				- tije						4.5	ije:	<b>_</b> ""	-				. tiine	-16-"					-10-200	in .		HIST RE					Author		
XNOR						giniti	لمحتوا				• •	- 10 <sup>2</sup>	i=1 ig	and a second	marks.			1 1 1 1 1 1 1	91 - 1 - P	and the second se				- 11			-	Y dila			Organization	1	
XOR								4.3															1					e tiin			Info		
sit				- Jun	يد ا	il action	()  (-)	- 16 C		15		Le ig	Linsfrid The Control		- 10 C		Jun		til miliki	<b>.</b>	1		- Fil		120	- e"					Page	Page0	
vittg				L(***	•	titestit							lun fiid						til mofid					86 C	- 163	20 C							
ND				-ter (Citize		· · · · · ·				10							16 Stilm		<u>a.                                    </u>														
NDtg						• • •					•								• • •														
r		~				· +																											
pen 💌	nstance P	ind																															
	_																																
	1.																																
																																	_
nbol:	+ + 4_BI	T_OR c	Comr	mand																													×
raries	Hierarchy		cell op	en -desi	gn 4bi	vedic	cell 2	NOR -	type se	chema	tic																						^
dy			cell op	en -desi en -desi	gn 4bil gn 4bil	vedic	cell 2	XNOR	-type :	schem	atic																						-
		here to			-		11t			-	-		-	-		-		Æ						_		Mos			~ 1		ENG	12:01	-



<u>File Edit View Dra</u>				- 8
그 🖻 🚅 🖬 🕼 🐰	ⓑ ◙ ◙ ፼ ፼ ፼ ፼ # → ॾ ⊉ ◙ • @ ♥ ● • . [▶] ◻ ◳ ▾ ! ○ । ↓ @ • . [ ㅍ + ↔ ● 秒  ▷ ▷ ○ ○ @   ≀	20 -		
🗸 🗸 🚓 🛠 🕨 🔳	12 y≥ i≥ a≥ IP 8.0:-0.5 inch v SELECT SELECT			
oraries 🥥 🛙	M HAschematic 2bit/HA_2	4 Þ 🗙	Properties	g
oitvedic ~			Schematic of HA	
www.edic *		•	10 × ± % %	1
itvedic 🔨			8. PBr 🔴 🕸	
_Pads			<ul> <li>System</li> </ul>	4bitvedic
gicGates ICE_Elements			Design Gell	HA
ICE_Elements			Type	schematic
Add Remove			Name	view0
er 🗸			Interface	view0
11 ^			RevisionCount	6
12			Date	8/17/2023 12:3
13			Version	
Abit		•	Author	
AbitTG		out:	Organization	
osmux			Info Page	Page0
a			Page	rageo
usingtg		•		
ladder oert_cell				
Sert_cell				
pen 💌 nstance Find				
pen	where $\int \frac{d}{dt} = \frac{1}{2} $			
and a second	Command			×
nbol: + > view0 of :				
oraries Hierarchy	point click 0 0.7 mode escape			^
dy	cell open -cell 2bit -design 4bitvedic -type schematic -context AND_1 -tracenets		ALL OF ENG	JM O



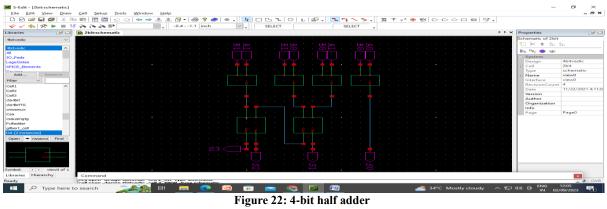


Figure 22 indicates the implemented 4-bit half adder.

그 & # # # * * * * * * * * * * * *	⇔ → ≛ ‡ ◙ + @ ? #   ● .   ┡ □ ╚ ┖   ○   ᢧ   ₽ .   ┖ ╹ ヽ ≶ .   巫 + ↔ ●	
🗸 🖌 🏤 🛠 🕨 🔳 👯 🍖 🍾 🗞 💷	-1.8 : -0.3 inch SELECT SELECT	
oraries 🖉 🖾 🚺 4_BIT_NAND:schem	atic	4 Þ 🗙 Properties 🥬
sitvedic ~		Schematic of 4_BIT_NAND
		10 × ± % %
Nitvedic ^		lk. Pec ● ₩
Pads		<ul> <li>System</li> </ul>
gicGates		Design 4bitvedic
CE_Elements	· · · · · · · · · · · · · · · · · · ·	Cell     4_BIT_NAND
		Type schematic
Add Remove		Name 4_BIT_OR
er 🗸		Interface view0
iDtg ^		RevisionCount 1
		Date 8/4/2023 6:30
· · · · · · · · · · · · · · · · · · ·	The second se	Version
IMUX		Author
2encoder		Organization
pit_and		Info
IT_NAND	a 🚥 🚽 📑 🕺 🖓 🖓	Page Page0
IT_NOR		
BIT_OR		
BIT_SRAM	(m + ).	
oit_sub 🗸		
en 💌 instance Find	New years of	
bol: ()		
raries Hierarchy Command		
	CORE OF A CAPE SCHEMACE	
P Type here to search		• · · · · · · · · · · · · · · · · · · ·

Figure 23:4-bit NAND.

Figure 23 represents the optimized 4-bit NAND.

<u>ile E</u> dit <u>V</u> iew <u>D</u> raw				- 6
יא  🛯 🖬 📽 בי		5 ° 🛷   • . 🖪 🗆 🗠 ٦   0   L   🖉 . 🔼 🥆 🔨 5 . 🗷 🕇	°° ● 🕅 🗅 🗇 🗘 🗂 💷 🖓 .	
/ 🗸 🚓 🛠 🕨 🔳 🕯	😵 🔊 🔊 🕸 🏴 🔤 🗸 -3.6 : 1.7	inch SELECT SELECT		
raries  😥 🗵	Magazine 4_BIT_NOR:schematic		4 ▷ 🗙	Properties 😥
itvedic ~				Schematic of 4_BIT_NOR
				10 × 1 95 95
itvedic ^				10 Per 🔴 🐨
Pads				System
picGates		Pitos z 56n		Design 4bitvedic
ICE_Elements				Cell     4_BIT_NOR
		· · · · · · · · · · · · · · · · · · ·		Type schematic
Add Remove				Name     4_BIT_OR
ter ~				Interface view0
NDtg ^				RevisionCount 0 Date 8/4/2023 6:30:
r i i i i i i i i i i i i i i i i i i i		· · · · · · · · · · · · · · · · · · ·		Version 0/4/2025 0:50:0
rtg		PR03_2 = } = \$ son	•••••••••••••••••••••••••••••••••••••••	Author
1MUX 2encoder				Organization
bit_and				Info
BIT_NAND				Page Page0
BIT_NOR		<b>PHO3</b> 1		
BIT_OR Cell: 4_BIT_NOR; Design:	· · · · · · · · · · · · · · · · · · ·			
Cell: 4_BIT_NOR; Design:	4bitvedic			
bit_sub v				
pen 🔻 instance Find				
		mtos s; findedes; findedes	· · · · · · · · · · · · · · · · · · ·	
		ՀՀՀՇՇՀՀ Աշղաքը Քին Աշղաքը Քին Աշղաքը շեն ՀՀ <mark>(</mark> )։ Աշղաքը շեն ՀՀՀ		
		· · · · · · · · · · · · · · · · · · ·		
ibol: + +	·····	······································		
raries Hierarchy	Command			×
dy	call open design thitvedic cell 2 VNOP -type sen	CHRICK.		10 N

# Figure 24:4-bit NOR.

Figure 23 represents the optimized 4-bit NOR.

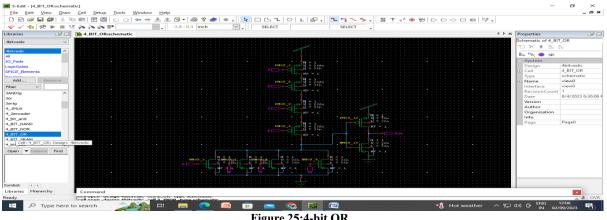
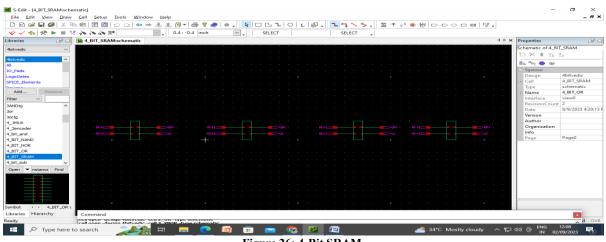
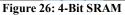
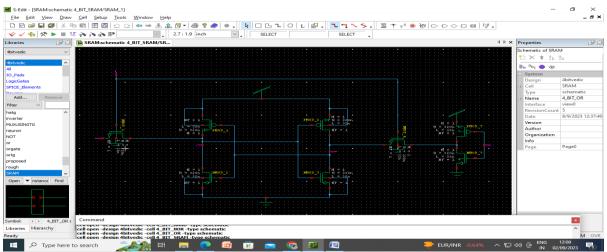


Figure 25:4-bit OR.

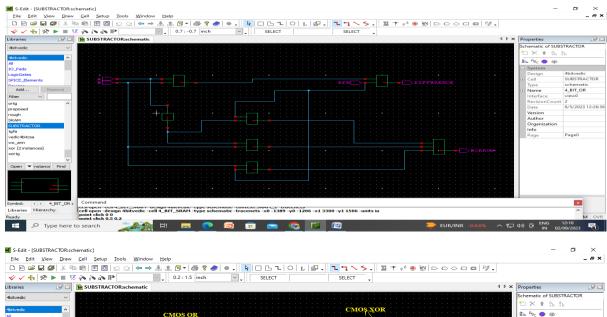
Figure 25 represents the optimized 4-bit NOR.

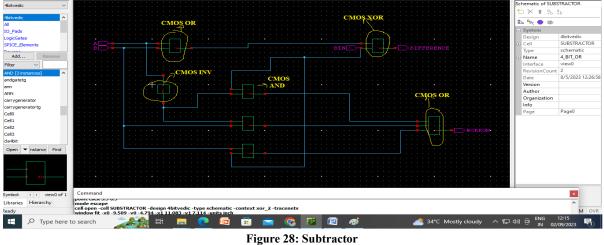




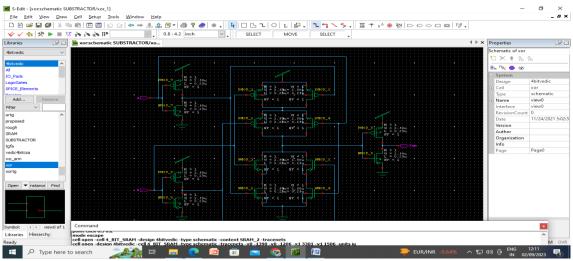








#### Figure 28: Subtractor





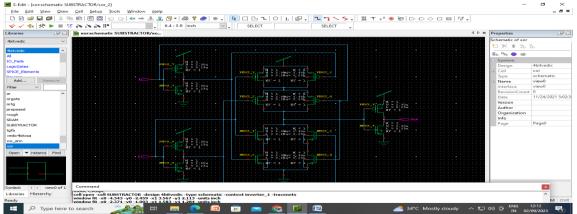


Figure 30: basic block of CMOS CMOS XOR in subtractor.

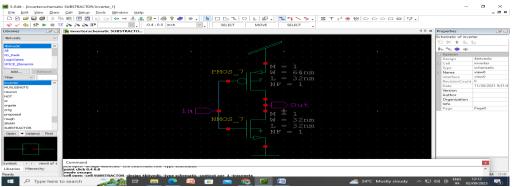
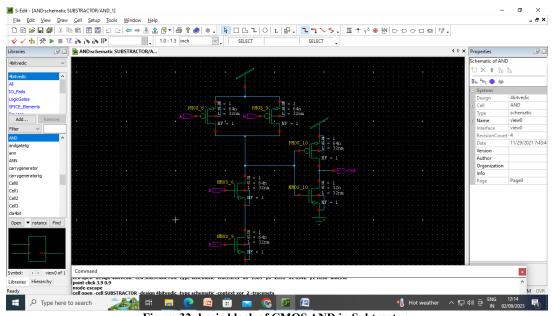
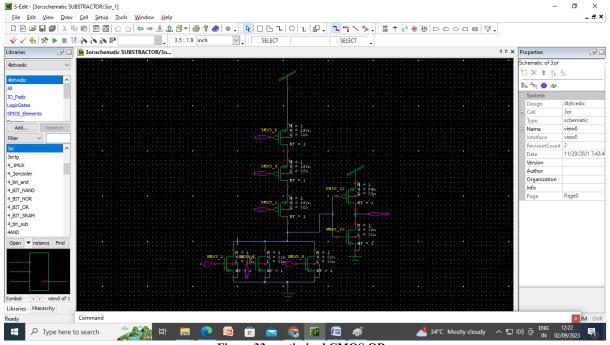


Figure 31: basic block of CMOS Inverter in Inverter.









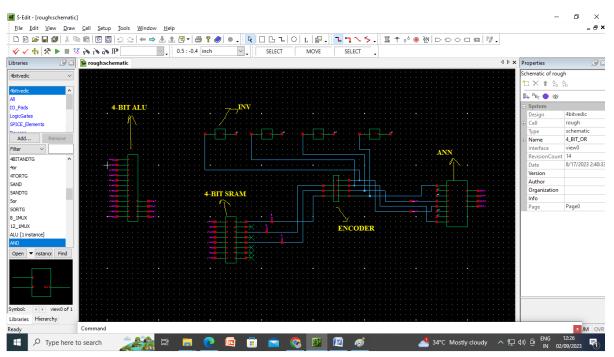


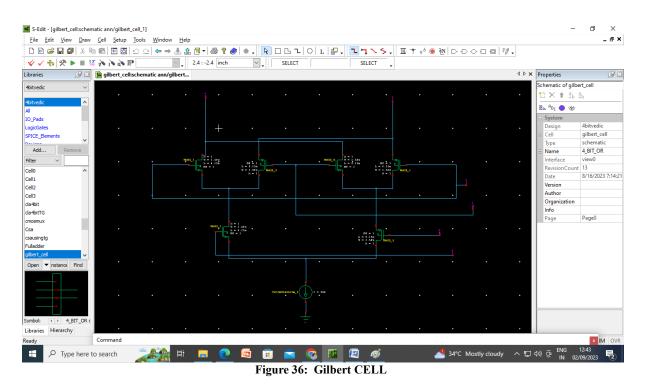
Figure 34: Basic 4-bit processor with ANN.

S-Edit - [ann:schematic] ٥ × \_ @ × <u>File Edit View Draw Cell Setup Tools Window Help</u> ✓ ✓ ♣ 😤 ► ■ 👯 ⋈ ⋈ № ~ **.** -3.7 : -4.3 inch SELECT SELECT 🏈 🖾 📔 ann:schematic 4 Properties Libraries Schematic of ann 4bitvedic C × ↑ % % 🛼 Agr 🥏 😸 IO\_Pads LogicGates SPICE\_Ele System i - t 4bitvedic Cell ann schematik Гуре Add.. 4\_BIT\_OR Name Filter view0 Revisio Date 23 12\_1MUX 8/17/2023 1:23:27 ALU AND Version Author indgatetg Organization Info ANN Page0 Page arrygen carrygeneratortg Cell0 Cell1 Cell2 Find Open 💌 nsta 4\_BIT\_OR Libraries Hierarchy Command × JM OV 🥕 🗷 😨 🧟 🛱 🖾 🖉 🖉 📥 34°C Mostly cloudy 🛛 스 토고 4%) 📴 🛯 IN . 

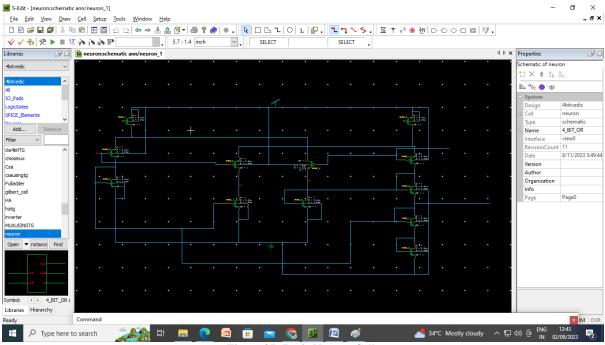
The sub-blocks are presented in figures 35, 36,37,38,39.

Figure 35: Basic structure of ANN using CMOS.

The above design depicted in fig 35 shows the ANN with basic CMOS blocks



As the multiplier block, the Gilbert cell is employed in the ANN circuitry. Four-quadrant multiplication is possible with the Gilbert multiplier cell, which is an alteration of the emitter coupled cell. As a result, it serves as the foundation for the majority of IC multipliers.





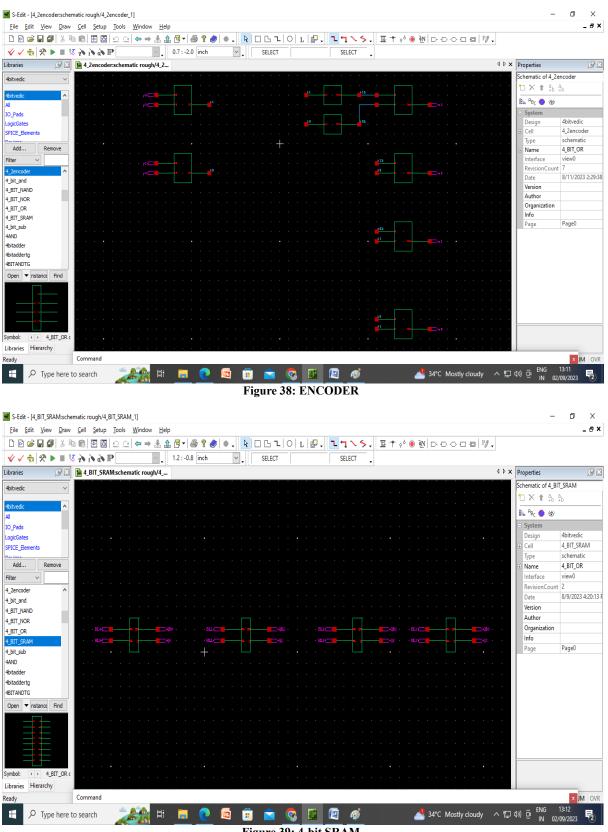


Figure 39: 4-bit SRAM

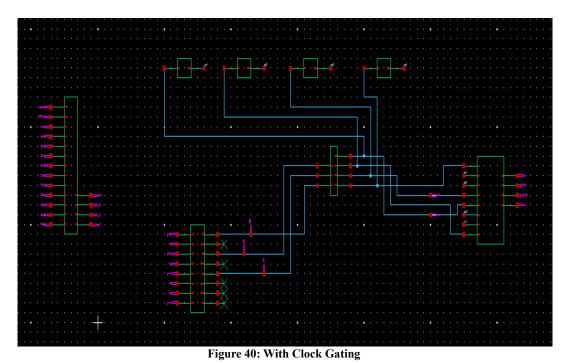




Figure 41: Simulation waveform with Clock Gating

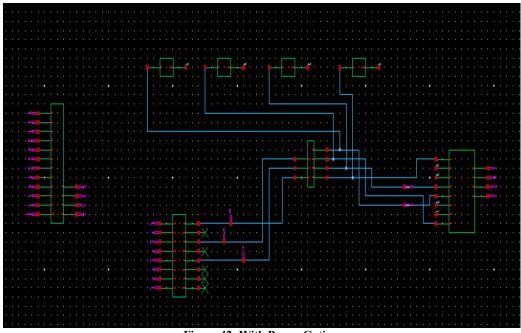


Figure 42: With Power Gating

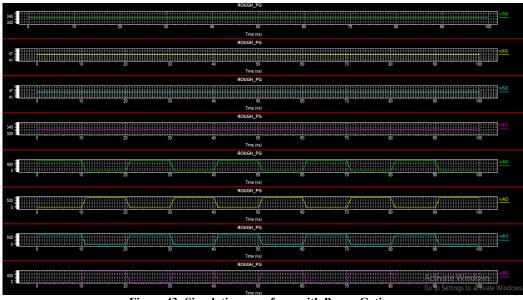


Figure 43: Simulation waveform with Power Gating

\* BEGIN NON-GRAPHICAL DATA

Power Results y1 from time 0 to 1e-007 Average power consumed -> 5.211081e-003 watts Max power 6.205597e-003 at time 4.07875e-008 Min power 4.930157e-003 at time 1.16345e-008

- \* END NON-GRAPHICAL DATA
- \* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

delay = not found Trigger = 1.0571e-008 Target = not found

\* END NON-GRAPHICAL DATA

Figure 44: Power Results with 45nm

\* BEGIN NON-GRAPHICAL DATA

Power Results

v1 from time 0 to 1e-007 Average power consumed -> 2.788101e-004 watts Max power 6.719861e-004 at time 7.08596e-008 Min power 1.081531e-004 at time 6.025e-008

\* END NON-GRAPHICAL DATA

\* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

delay = 6.8672e-011 Trigger = 1.0571e-008 Figure 45: Power values with 32nm

# **CONCLUSION:**

Below tables represents the comparison of area and power values of the proposed design.

SL.NO	TECHNIQUE	NO OF MOSETS	POWER
1	WITHOUT ANN	880	2.788101e-004W
2	WITHOUT ANN_CG	1048	4.489172e-006W
3	WITHOUT ANN_PG	1048	2.155765e-004W
F			
SL.NO	TECHNIQUE	NO OF MOSETS	POWER
<b>SL.NO</b>	TECHNIQUE WITH ANN	<b>NO OF MOSETS</b> 1380	POWER 6.044845e-004W
SL.NO           1           2	-		

With the above results we can conclude that for the proposed result with and without CG,PG, ANN we got prominent results when compared with existing approaches<sup>1,2,3,4,13,15</sup>. The circuit blocks of design are represented. Clock gating is a power optimization technique commonly used in digital circuit design, including Arithmetic Logic Units . The primary goal of clock gating is to reduce power consumption by selectively disabling the clock signal to certain circuit elements when they are not actively needed. Clock gating can be applied to specific parts of the unit to minimize power consumption during idle or low-activity periods, based on the current operation requirements. The clock gating logic operates dynamically based on the ALU's current state and the specific operation being executed. When the ALU is idle or waiting for a new operation, clock gating can be applied to reduce power consumption during these periods. By selectively disabling the clock to parts of the ALU when they are not needed, power consumption is reduced. CG introduces additional complexity to the design. Power gating involves inserting switches into the power supply lines of specific circuit blocks. When a particular block is not actively needed, the power switch is turned off, disconnecting the power supply and isolating the block from the rest of the circuit. In the work<sup>15</sup> the power dissipationed was 0.1541nw, in [13] it is 5.9414mw

### **REFERENCES:**

- 1. Sujata. A.A, Lalitha. Y.S, "Design and performance analysis of 4-bit Nano-Processor design for low area, low power and minimum delay using 32nm FinFET technology", WSEAS TRANSACTIONS on ELECTRONICS, DOI: 10.37394/232017.2021.12.1
- 2. K. Prasad Babu, Dr. K.E. Sreenivasa Murthy, Dr. M.N. Giri Prasad, "Design of CMOS Digital-Processor using Hybrid Technique", 10.1109/ICACCS51430.2021.9441689, IEEEXPLORE.
- K. Prasad Babu, Dr. K.E. Sreenivasa Murthy, Dr. M.N. Giri Prasad, "Design of CMOS Digital-Processor Using Clock Gating", vol1,2022, TELEMATIQUE Pg.No.2488 – 2510, ISSN: 1856-4194

- 4. K. Prasad Babu, Dr. K.E. Sreenivasa Murthy, Dr. M.N. Giri Prasad, "Implementation of Power Gated Alu For Low Power Processor", Journal BIOGECKO (ISSN: 2230-5807), Vol 12 Issue 01 2023, Pg.No: 765-780.
- 5. DALIA EL-DIB, et.at, "Procedures of Low Power Digital Design: A Survey", Wseas
- 6. Transactions On Electronics, E-ISSN: 2415-1513, Volume 9, 2018.
- Aqilah binti Abdul Tahrim,et.al, "Plan and Performance Analysis of 1-Bit FinFET Full Adder Cells for Subthreshold Region at 16 nm Process Technology", Hindawi Publishing Corporation Journal of Nanomaterials, Volume 2015, Article ID 726175. 13 pages, http://dx.doi.org/10.1155/2015/726175.
- 8. Debajit Bhattacharya,at.al, "FinFETs: From Devices to Architectures", Hindawi Publishing Corporation, Advances in Electronics, Volume 2014, Article ID 365689, 21 pages, http://dx.doi.org/10.1155/2014/365689.
- G.Saranya, R.S. Kiruthika Optimized Design Of An Alu Block Using Architectural Level Of Power Optimization Techniques 3/1/2011 IEEE XPLORE 168-172.
- 10. Jinhui Wang, Na Gong Pns-Fcr:Flexible Charge Recycling Dynamic Circuit Technique For Low Power Microprocessors 2/1/2016 Ieee Transactions On Vlsi Vol 24 No.2 613-624.
- 11. A J Ryan Philips "4-Bit Microprocessor: Design, Simulation, Fabrication, and Testing"Volume 18, Issue 1 (2009) Microelectronic Engineering Conference 2009, pages 81-91.
- 12. Suchismita Sengupta, Partha Sarkar, Ananya Dastidar, "Design of a 4 Bit Arithmetic & Logic Unit, Evaluation of Its Performance Metrics & its Implementation in a Processor",
- 13. 978-1-7281-6221-8/20/\$31.00 ©2020 IEEE, Pg.No: 1-8.
- Wenheng Ma, Qiao Cheng, Yudi Gao, Lan Xu and Ningmei Yu, "An Ultra-Low-Power Embedded Processor with Variable Micro-Architecture", Micromachines 2021, 12, 292. https://doi.org/10.3390/mi12030292. P.g. No: 1-16.
- Vegha. B N, Dr. Vijay Prakash, "Design and Implementation of 4-Bit ALU for Low-Power using Adiabatic Logic based on FINFET", International Journal of Engineering Research & Technology (IJERT), ISSN: 2278-0181, Vol. 9 Issue 07, July-2020, Pg. No: 649-656.
- JunHa Suk, ChanYeop Ahn, S M Mojahidul Ahsan and SoYoung Kim, "A stable 4-bit ALU design for printed devices", Flexible and Printed Electronics, Vol7, Number 1, DOI 10.1088/2058-8585/ac49da, ISSN: 2058-8585,
- Mary Sajin Sanju.I, M. Vadivel, "Performance Evaluation of an Efficient ALU", Nanotechnology Perceptions 19 No.2 (2023) 10–18, ISSN 1660-6795.
- K.Prasad Babu, Dr. K.E. Sreenivasa Murthy, Dr. M.N. Giri Prasad, "A Study & Analysis on low Power processor Design Using Various Techniques", Jornal of propulsion technology, ISSN:1001-4055, vol 44, no 3 2023, pg no :2355-2379.

## **BIBLIOGRAPHY:**



K Prasad Babu is working as an Associate Professor in the department of Electronics and Communication Engineering of Ashoka Women's Engineering College, Kurnool, Andhra Pradesh, India. He has 15 years of Teaching experience. He has received his B.Tech degree in 2002, M.Tech degree in 2007. Currently he is pursuing PhD in the area of VLSIDesign, JNTUA College of Engineering, Anantapur, Andhra Pradesh, His areas of interest includes VLSI, Embedded Systems, Image Processing. He has published several papers in conferences national & international and in national & international journals.



Dr. K.E.Srinivasa Murthy is currently working as Principal, Ravindra College of Engineering for Women, Kurnool, Andhra Pradesh, India. In the year 1989, K.E.Sreenivasa Murthy completed his B.Tech from S.V.University, Andhra Pradesh, In the year 1992 he finished M.Tech from S.V.University, Andhra Pradesh. In 2003 he obtained the PhD degree from S.K.University, Andhra Pradesh Overall experience in teaching is 28 years. His areas of interest include Embedded systems, Microcontrollers. He authored several national, international journals and conference manuscripts. He is life time member of ISTE and Instrumentation Society of India. He is member of IEE and IETE. He received lifetime achievement award from AIMER SOCIETY. He received Best Principal award for his efforts in developing the college.



Dr M.N. Giri Prasad is working as Adjunct Professor in the Department of Electronics and Communication Engineering at JNTUA College of Engineering, Anantapur, Andhra Pradesh, India. He worked as Director of Academics & Audit, JNTUA and various key positions. He has done various Sponsered projects by UGC. He received his B.Tech degree from JNTU College of Engineering, Anantapur, Andhra Pradesh, India in the year 1982, M. Tech degree from Sri Venkateswara University, Tirupati, Andhra Pradesh, India in the year 1994, and PhD degree from J.N.T University, Hyderabad, Andhra Pradesh, India in 2003. He is having more than 30 years of teaching experience. His research areas are Wireless Communications, Biomedical Instrumentation, signal processing, Image processing, embedded systems and microcontrollers. He has published around 60 papers in national and international conferences. Around 50 papers published in national and international journals. He is a life member of ISTE, IEI and NAFEN.