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Article

Simulation Of Optimized Low Power Cmos Digital Processor Design Using 32nm Technology

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ABSTRACT: In this work a CMOS based 4-bit processor is implemented with and without ANN. The foundry technologies used are 90nm, 45nm, 32nm. The simulations are performed and the power results along with no of MOSFETS are mentioned. The proposed work obtained promising results when compared with previous works. Nano processors utilize advanced fabrication techniques to create transistors and other components with nanoscale dimensions. These transistors can operate in conditions where classical physics laws may no longer directly apply and quantum effects can become significant. This introduces new challenges and opportunities for computing. In this research work, implementation of a 4-bit nano-processor utilizing Tanner Electronic Design Automation tool is proposed. The processor is developed using a cutting-edge 90nm, 45nm, 32nm technology files, focusing on achieving compactness, low power consumption, and efficient performance. The design process encompasses various stages, including schematic capture, simulation, and power analysis. The proposed Nano processor begins with a 4bit ALU that incorporates all fundamental and universal gates, an efficient and high-speed adder, multiplier, and multiplexer. The major subcomponents that can be changed are the Carry Save Adder and the multiplier. Power consumption and area reduction is optimised. The proposed Nano processor's second component is a 4-bit 6T SRAM, encoder and decoder, and an Artificial Neural Network. All of these subcomponents are created at the transistor level. Nano processors refer to a class of extremely small-scale integrated circuits designed to perform computation at the nanometre scale. The simulation results show for 90nm, power dissipation of 0.7009451 µW. For 45nm, power dissipation of 0.05211081µW. For 32nm, power dissipation of 0.0278810µW. With Power gating technique the obtained power is 0.05344917µw when compared with existing result. With Clock gating technique 6.044895 µW.

Keywords: Low Power, 4-bit Nano-Processor, 90nm, 45nm, 32nm, Power consumption, Power-Gating, Clock-Gating, ANN

INTRODUCTION

The development of nano processors could lead to significant advancements in various fields such as discussed in below:
1. Miniaturization: Nano processors enable the creation of incredibly small computing devices that can be embedded in everyday objects, leading to the proliferation of Internet of Things (IoT) devices and smart technologies.
2. High Performance: The smaller size of transistors in nano processors can potentially lead to faster and more energy-efficient computations, pushing the boundaries of computational power.
3. Quantum Computing: At the extreme nanoscale, quantum effects become prominent. Quantum processors exploit these effects to perform certain types of computations that are exponentially faster than classical computers for specific problems.
4. Biomedical Applications: Nano processors can be used in medical devices, drug delivery systems, and even inside the human body for various diagnostic and therapeutic purposes.
5. Energy Efficiency: As transistors become smaller, they typically consume less power, potentially leading to more energy-efficient computing systems.

However, developing and manufacturing nano processors comes with numerous challenges, including managing heat dissipation, dealing with quantum effects, and designing reliable components at such a small scale.4-bit Nano-Processor in this term "4-bit" suggests that the processor deals with data in 4-bit values. In computing, the number of bits in a processor's

data path influences its capabilities and limitations. A 4-bit processor would typically handle relatively simple tasks due to its limited data width. Low Area, Low Power, and Minimum Delay These are the key goals of the design. "Low area" refers to the desire for the processor's physical size to be minimized. "Low power" signifies an emphasis on energy efficiency, aiming to reduce the amount of power the processor consumes. "Minimum delay" implies a focus on optimizing the speed of the processor's operations. The study would involve both the theoretical design of the processor's architecture and the practical implementation using the specified technology. The subsequent performance analysis would assess how well the processor meets its design goals and may involve simulations, measurements, and comparisons with other processor designs. The design focuses on achieving low physical size, minimal power consumption, and fast operation. This includes optimizing the processor's architecture for these goals. The performance analysis assesses how well the design meets these objectives by measuring its area usage, power efficiency, and operational delay. The research paper aims to demonstrate the feasibility of a highly efficient and compact 4-bit processor using CMOS technology. The power in CMOS circuits is dynamic & static power dissipation. The dynamic power equation is given by $P_{dyn}=1/2\ C{\cdot}V^2{\cdot}f$, where C is the total capacitance that is being switched per clock cycle.V is supply voltage, f is the clock frequency. The Leakage power is given by $P_{leak}= I_{leak}$ V, where I_{leak} is the leakage current. V is supply voltage.

LITERATURE SURVEY:

Many authors contributed much of their focus on low power design of digital processor, a few of the represented here. In [1], the authors proposed 4-bit nano processor with FINFET technology, with power dissipations of 2.68µw (without ANN) and 1.98µw (with ANN), overall design was 314.4µW for 32-nm. In[2], authors mentioned about using the combination of CG & PG for 4-bit digital processor with power dissipation of 0.147mw (45nm), 2.375mw(90nm). In [3], authors mentioned about usage of CG for 4-bit digital Processor with the value of 233µw (45nm). In [4], authors have represented the design of power gated ALU, with power as 2.15 µw. In[5], the authors have discussed about the low power digital design survey. In [6], the authors contributed about the 1-bit finfet FA cells using 16nm. In [7], the authors have elaborated about the Finfets & its architectures. In [8], authors have presented optimization ALU with power gating technique. In [9], authors have contributed on dynamic circuit technique for low power processor design. In [10], author represented about the design & fabrication of 4-bit processor. In [11], authors evaluated the performance of 4-bit ALU with power value of 1.759 mw. In [12], the authors worked for power consumption of embedded processors & proposed 3 operating modes High-Performance mode, Normal mode, Low-power mode. The average amounts of power consumed by the respective modes are 41.7 µW, 59.7 µW and 71.1 µW. In[13], 5.9414mw. In[14], the authors has represented a stable 4-bit arithmetic logic unit (ALU) design using a minimum number of transistors that can overcome the limitations of printed devices. In [15], the authors proposed the 4-Bit ALU designed using the full-swing GDI technique, with power dissipation as 0.1541nw as average power. In [16], the authors represented the study and analysis of various contributions towards low power processor design techniques.

Proposed Design:

This section deals with the proposed 4bit nano processor design methodology & block representation. The proposed design differs from existing approach[1] with the usage of CMOS gates instead of FinFet, Usage of basic gates and optimised gates. The entire work is distributed as Basic design with CMOS gates, without ANN, CG,PG & with optimised CMOS gates, with ANN, CG & PG. The results are simulated using 90nm technology file, 45nm technology library file and 32nm library file. The important blocks in the design are 4-bit ALU which is composed of mux based. The SRAM circuitry is simulated single bit & 4-bit with and without CG,PG. In the work of the author[11] both analog & digital ALU were implemented and the power dissipated values were 1759µw, 5.360 µw respectively. In [13], the authors got the power value as 23.93mw with FInFET transistors. All the designs are operated with a supply voltage of 0.07 - 1.2v. In the existing method[1] the author used fingering concept, which engage in improvement the resistance of the gate poly terminal along the width of the transistor. With this technique the area and capacitance can be enhanced. Dynamic Power Consumption is associated with the charging and discharging of capacitors during switching. Primarily occurs during active operation when the circuit is actively processing data or executing instructions and directly related to the frequency of clock signals and the rate of switching. Static Power Consumption happens from leakage currents in transistors even when they are not actively switching. It is present during both active and idle states, contributing to power consumption even when the circuit is not performing computations and becomes more significant in advanced semiconductor technologies with smaller feature sizes and lower threshold voltages.

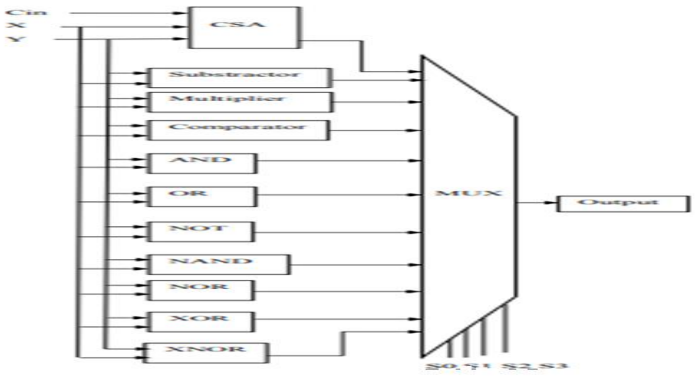


Fig A: Architecture of 4bit ALU with Input-combination of 11 MUX

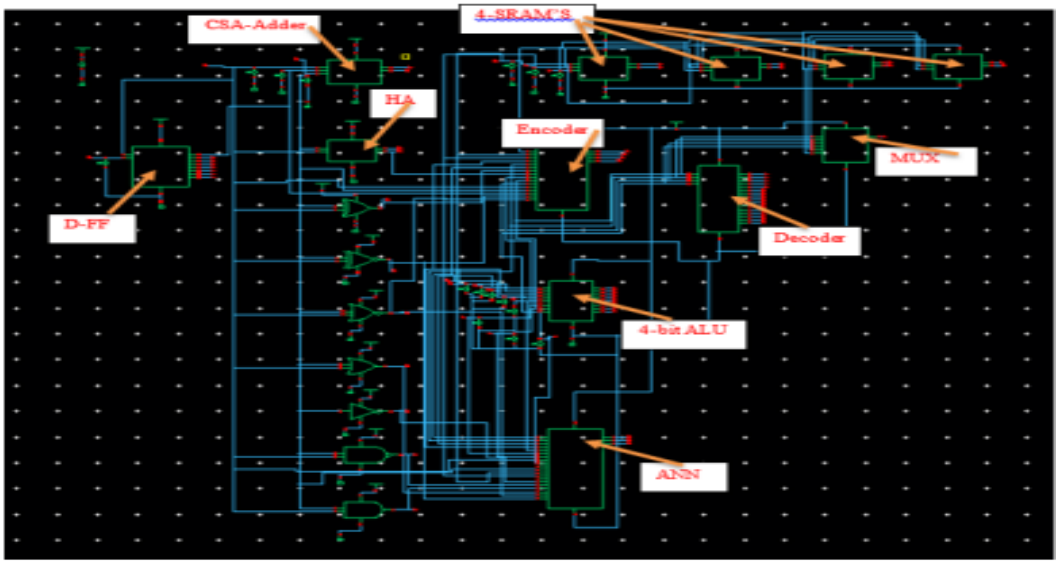


Fig B - Schematic of Existing 4 bit nano processor design

Figure B depicts about the existing system design of the design.

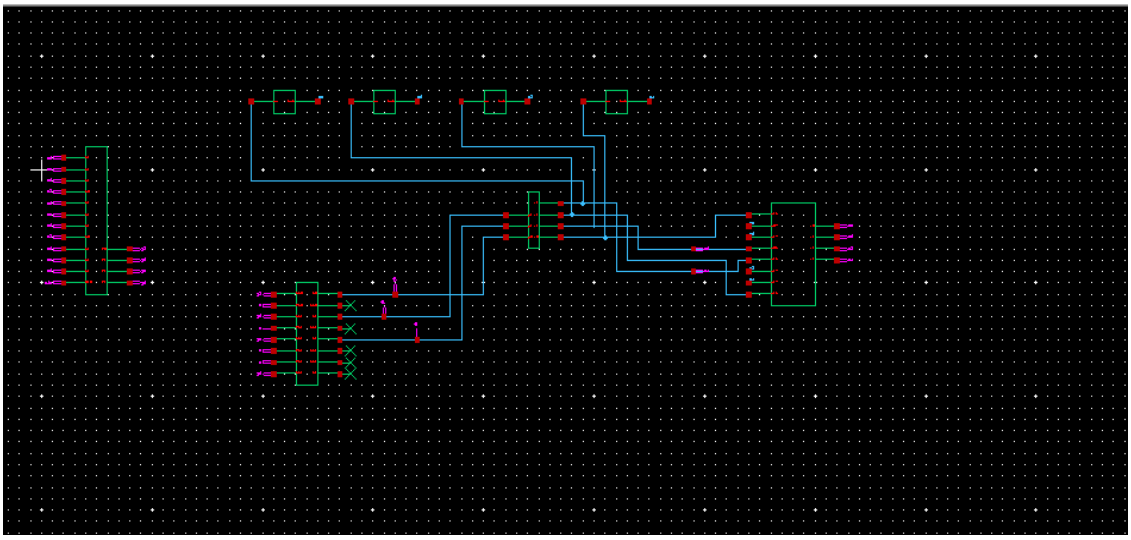


Fig C - Schematic of Proposed 4 bit nano processor design

To simplify the architecture, the processor is represented with the basic ALU, Encoder Decoder & ANN block as shown in figure C.

Simulation Results:
All the results are simulated using tanner EDA tool. The technology library files used are 90nm, 45nm, 32nm.

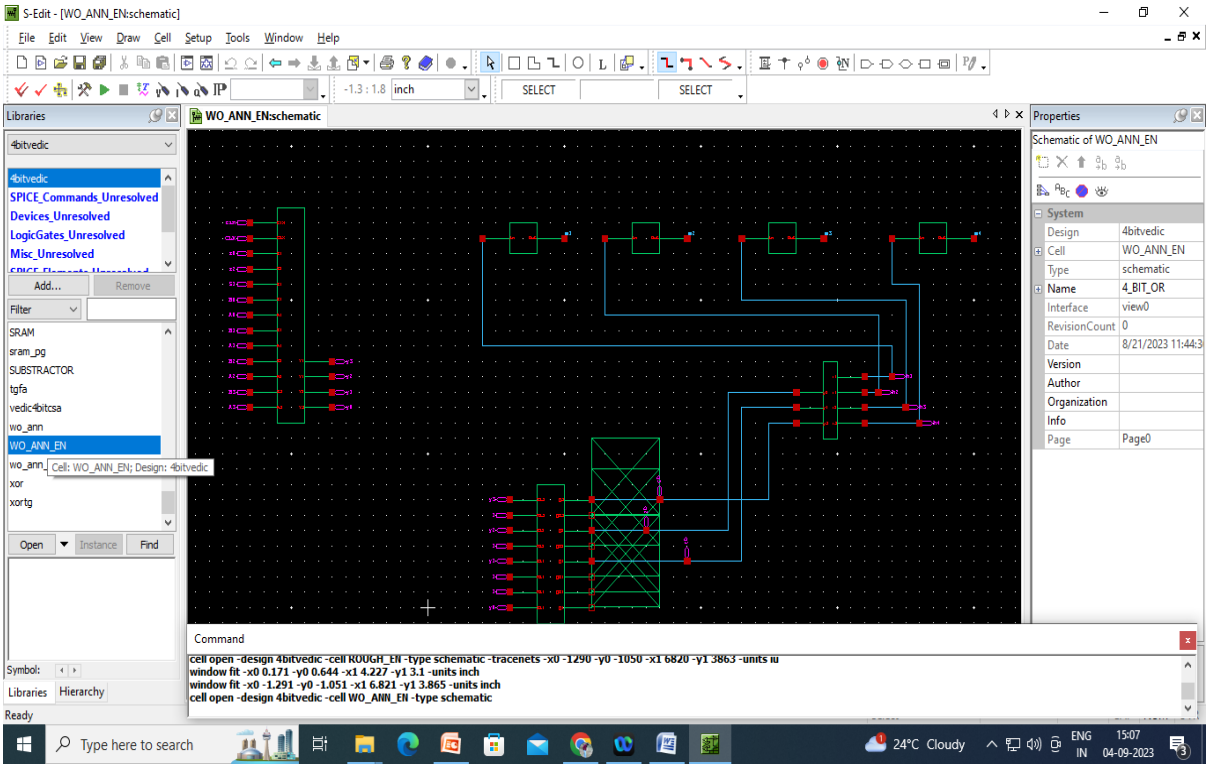


Fig 1: Without ANN schematic of proposed design

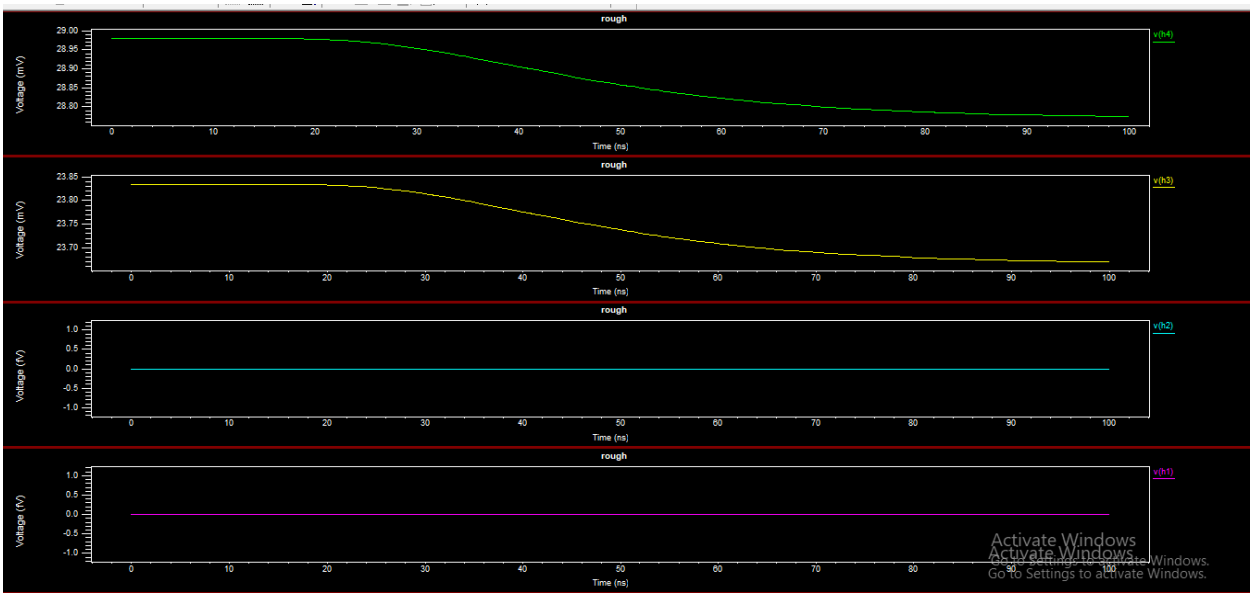


Fig 2: Waveform for Proposed 4 bit nano processor design

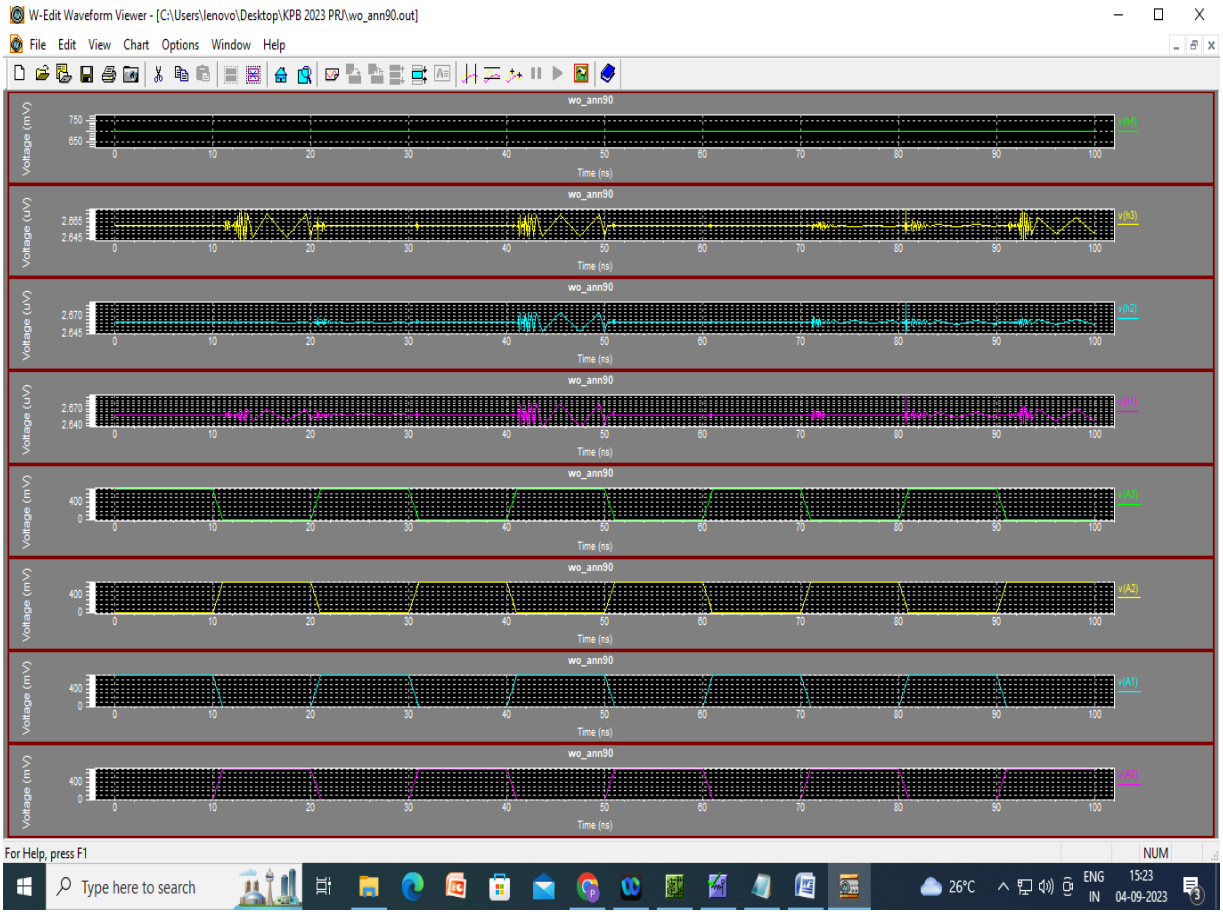


Fig 3: 90nm simulation

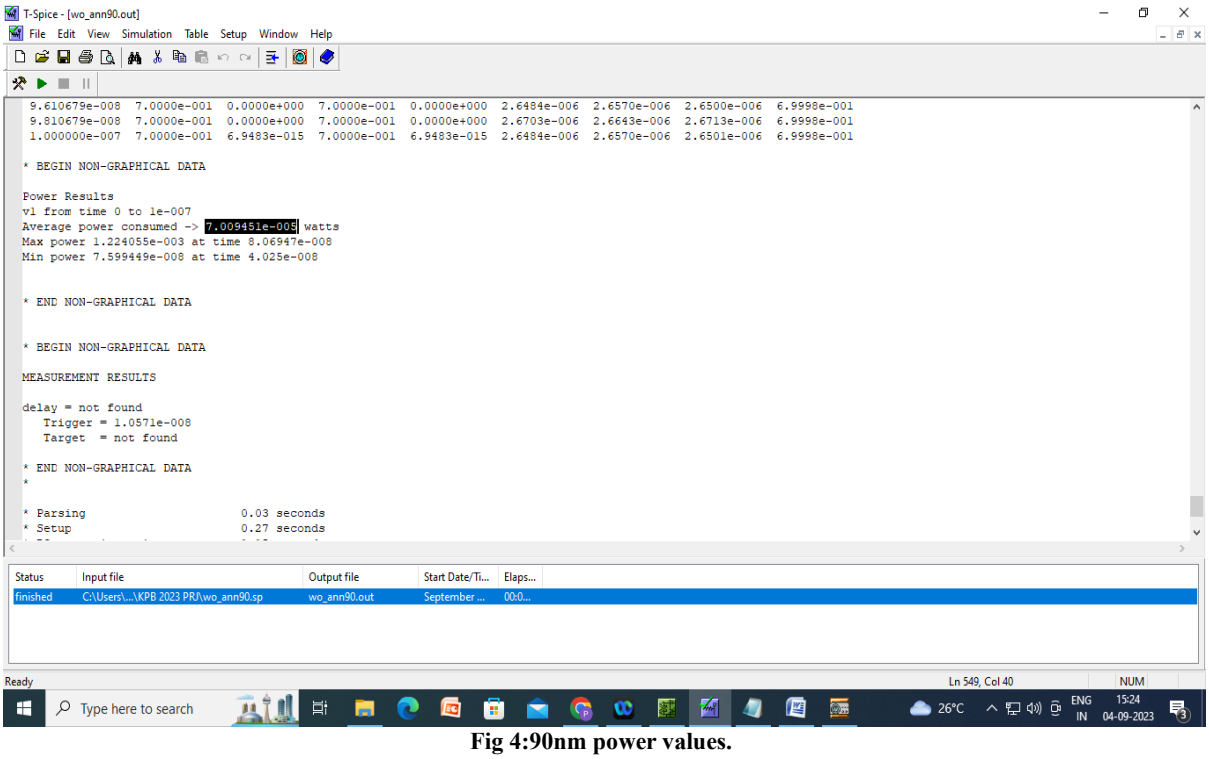


Fig 4:90nm power values.

Fig 4 shows the power value of 1.224mw maximum and average power of 0.1224µW using 90nm technology.

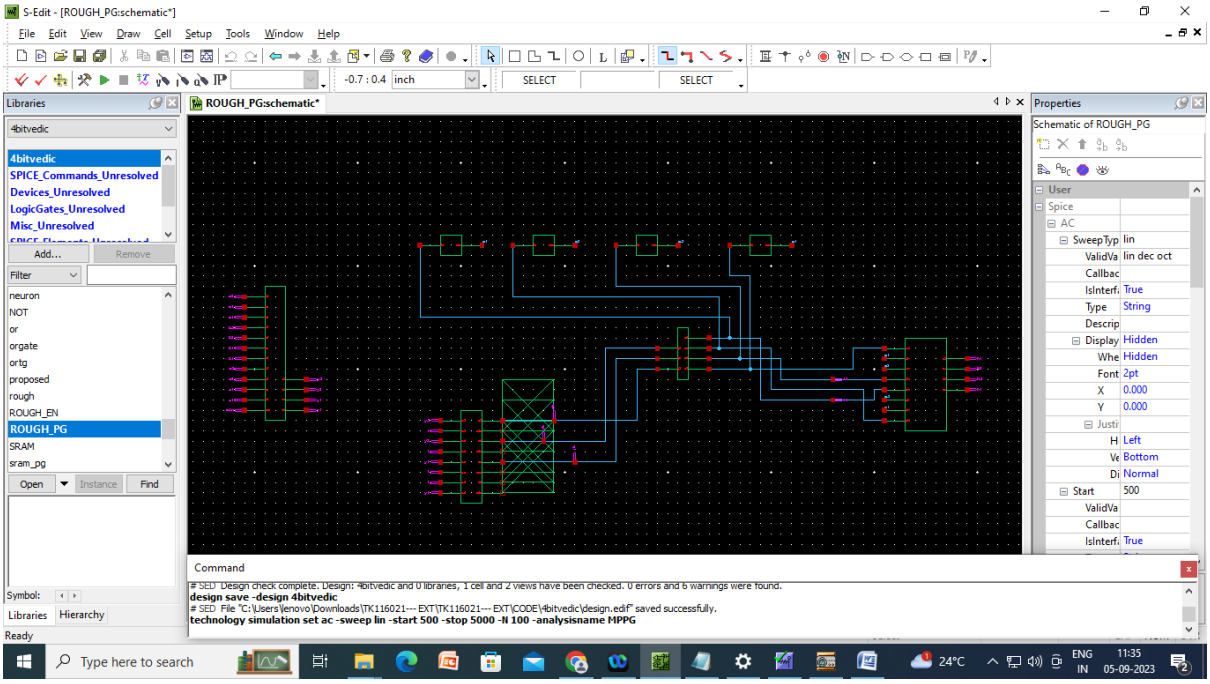


Fig 5 : 4-bit processor with power gating

Fig 5 indicates the PG technique employed for power reduction of the proposed design.

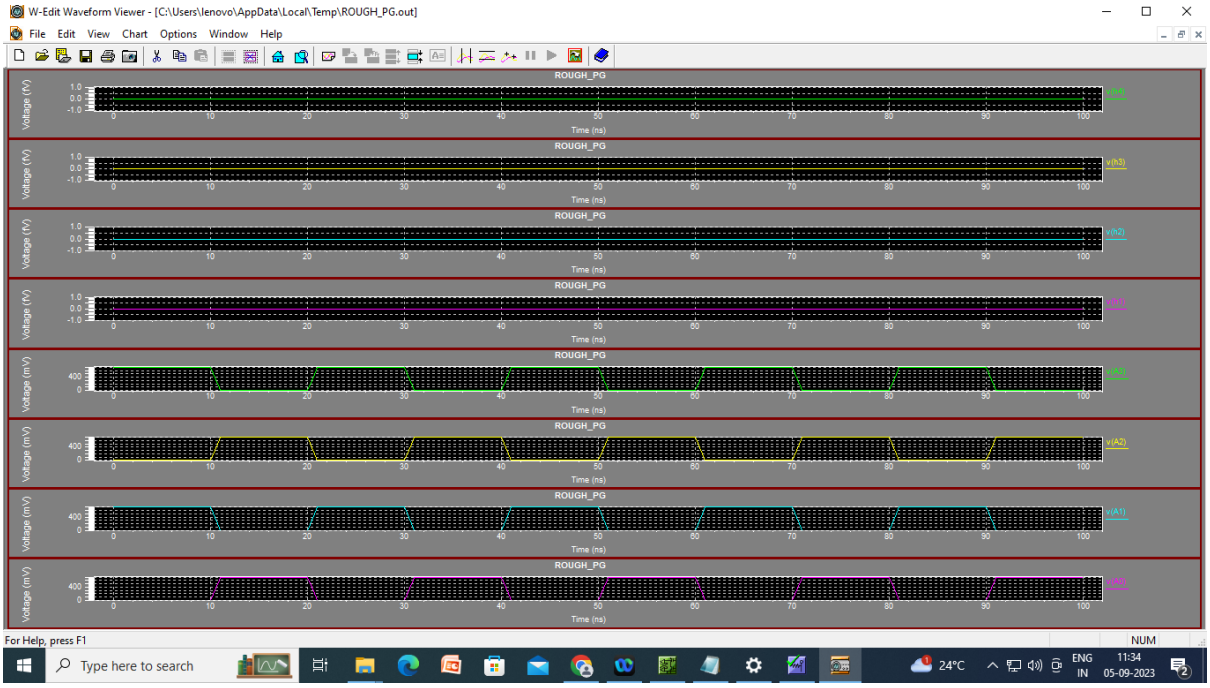


Fig 6: simulation of power gating

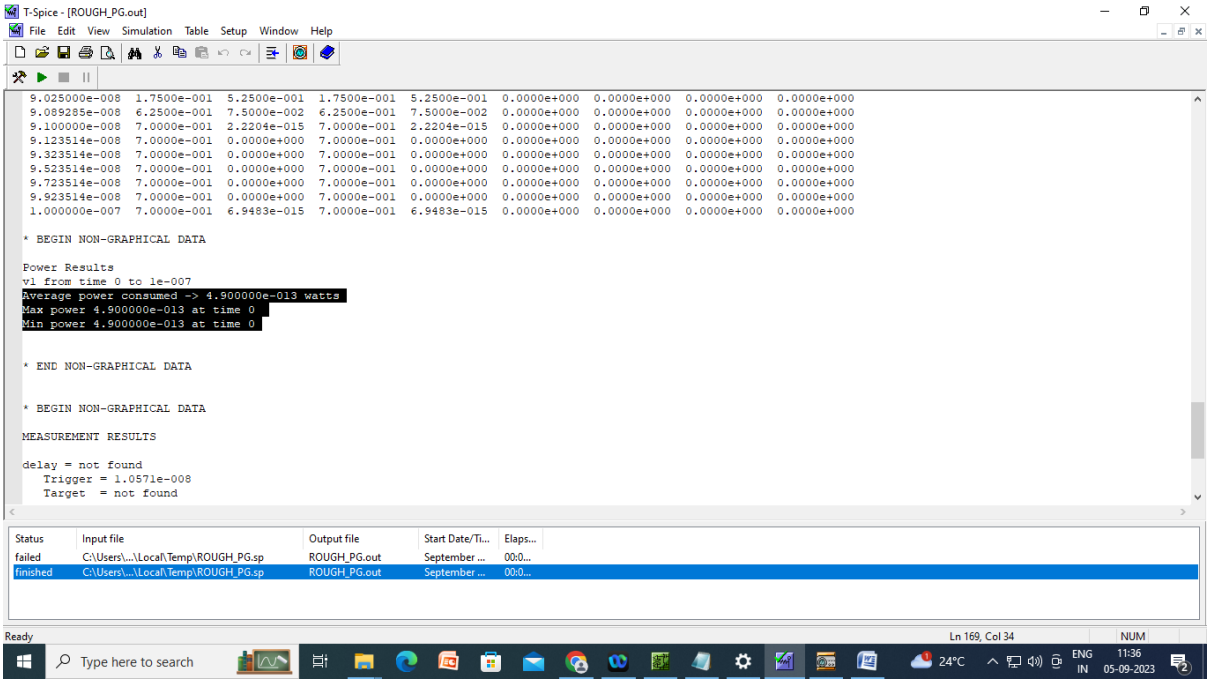


Fig 7: Power values of power gating

In the figure 7 the max power obtained is 49000 nw which is very less when compared with the existing system design of 314.4 µw

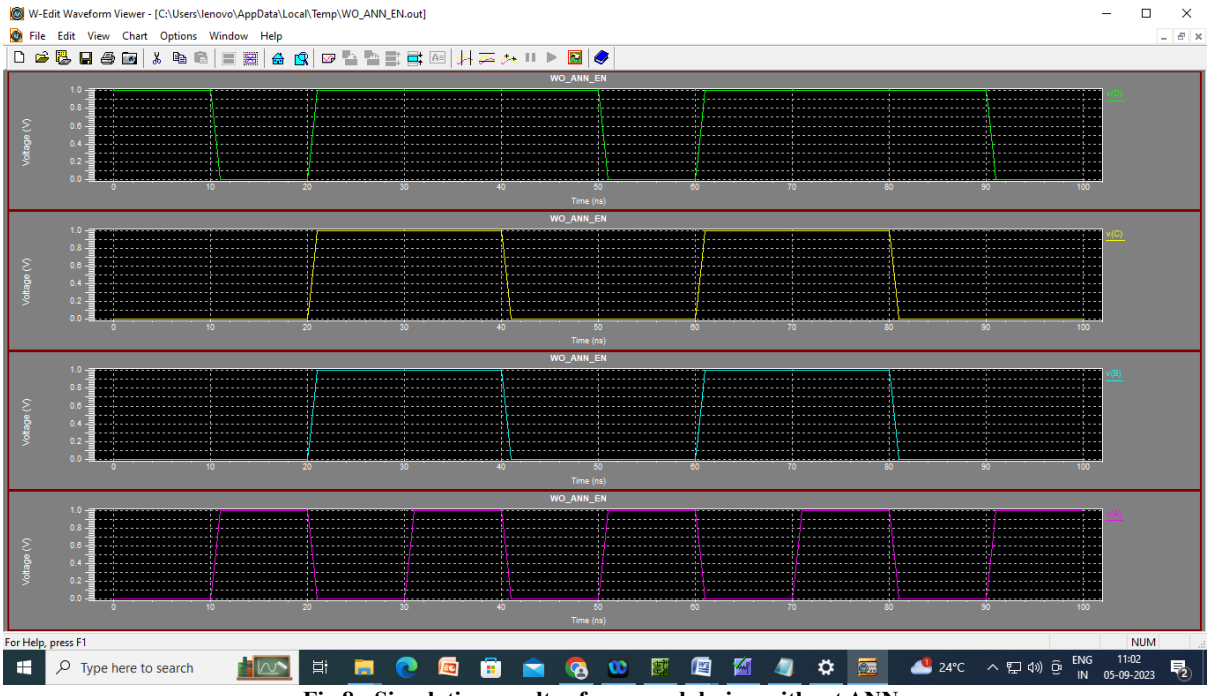


Fig 8 : Simulation results of proposed design without ANN

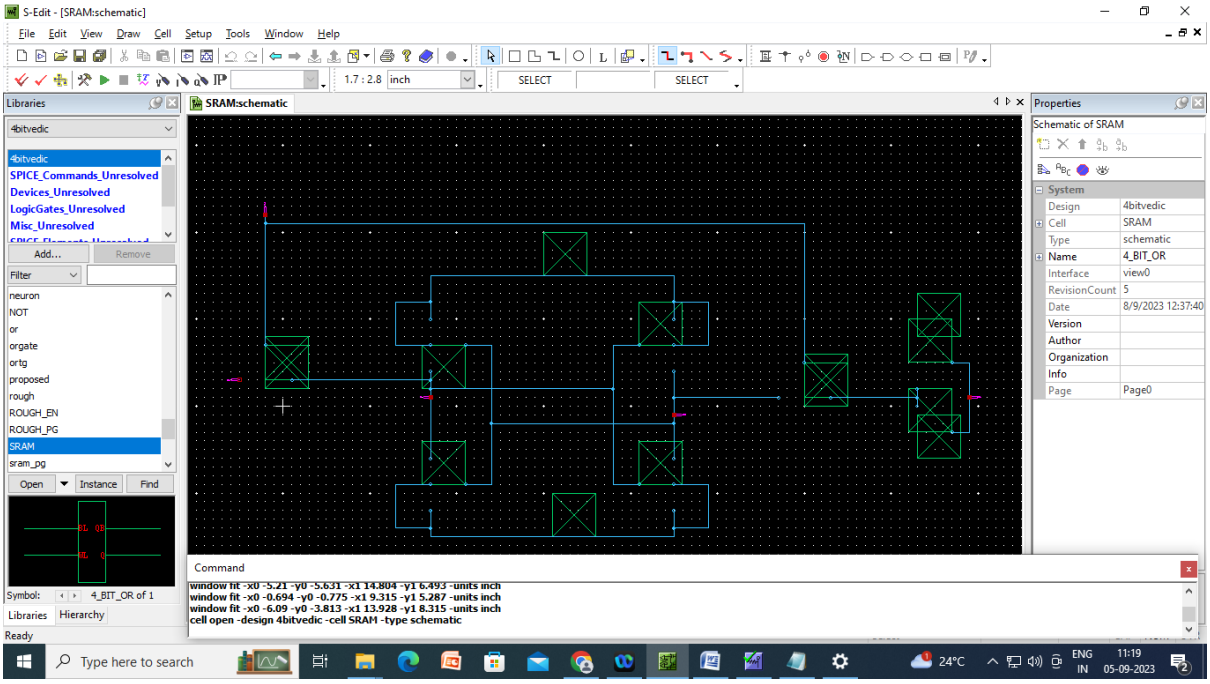


Fig 9: Internal Schematic of SRAM without PG

The SRAM internal schematic of the basic SRAM circuit is presented in figure 9.

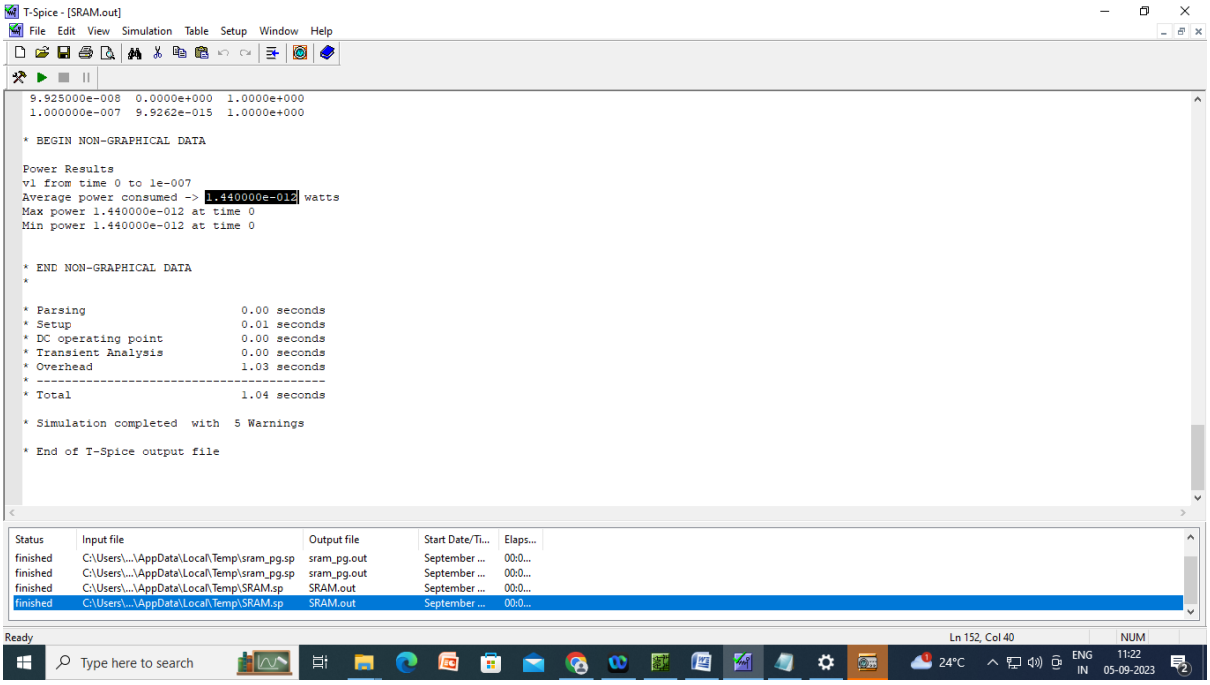


Fig 10: Power values of SRAM without PG

Basic SRAM circuit without PG is dissipating a value of 1.44 pw as shown in figure 10.

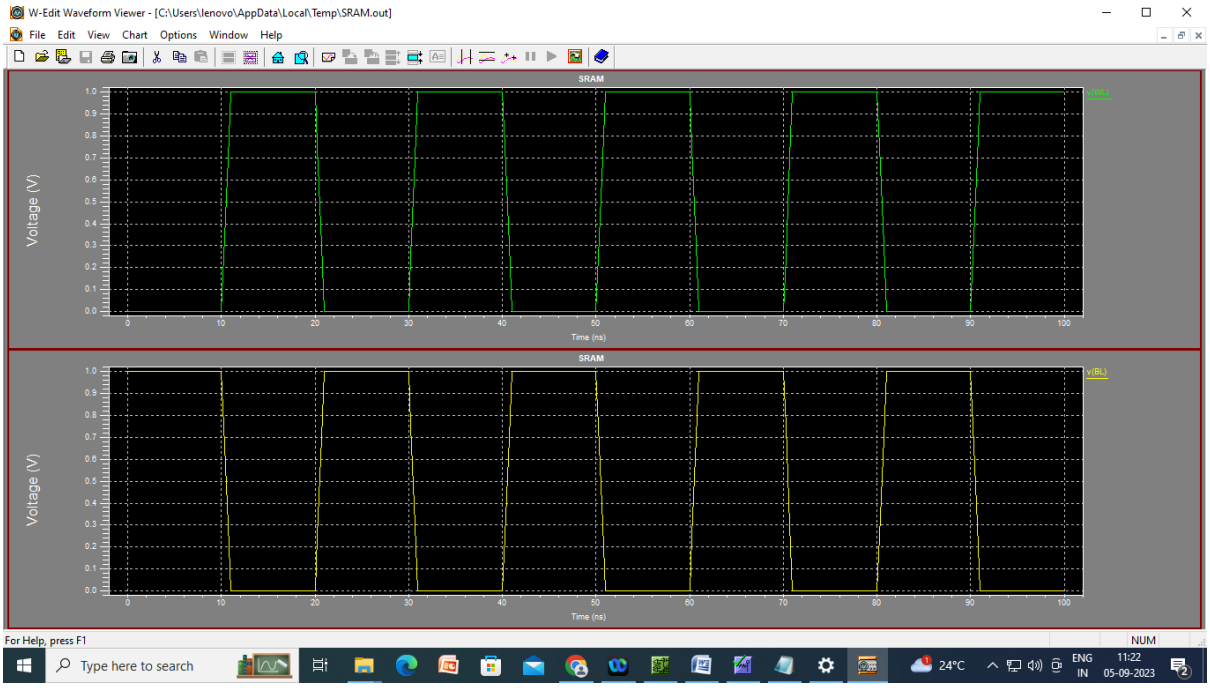


Fig 11: Simulation wave form of SRAM without PG

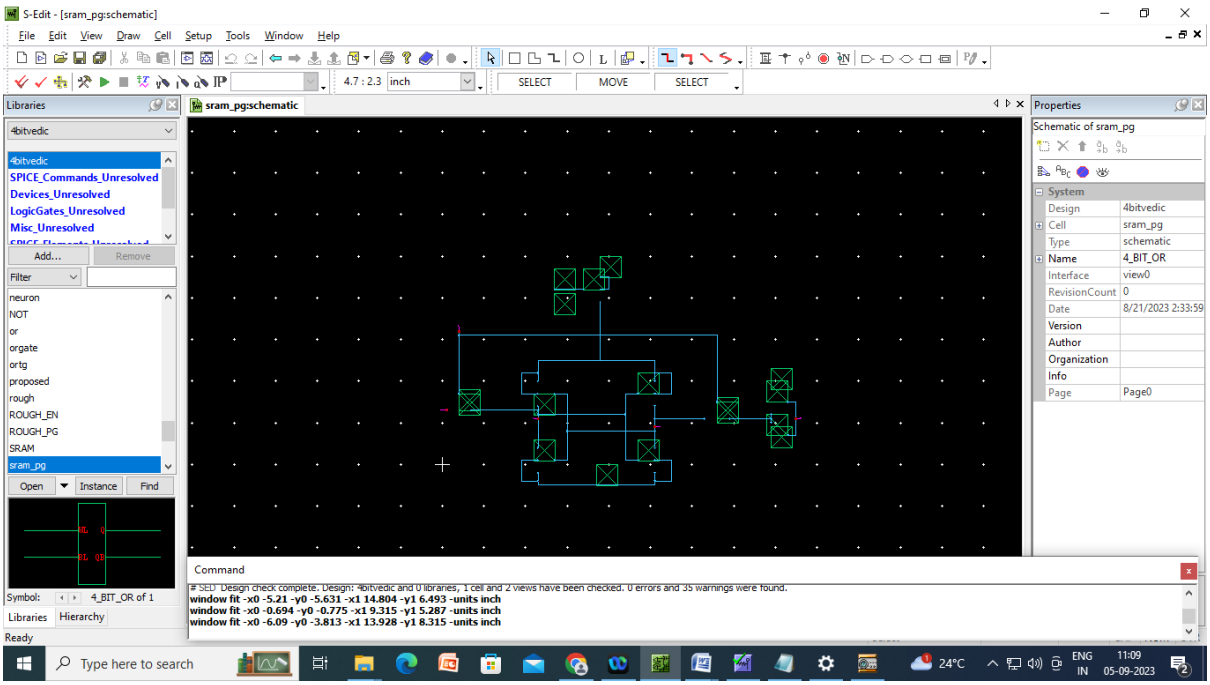


Fig 12 : SRAM schematic with PG

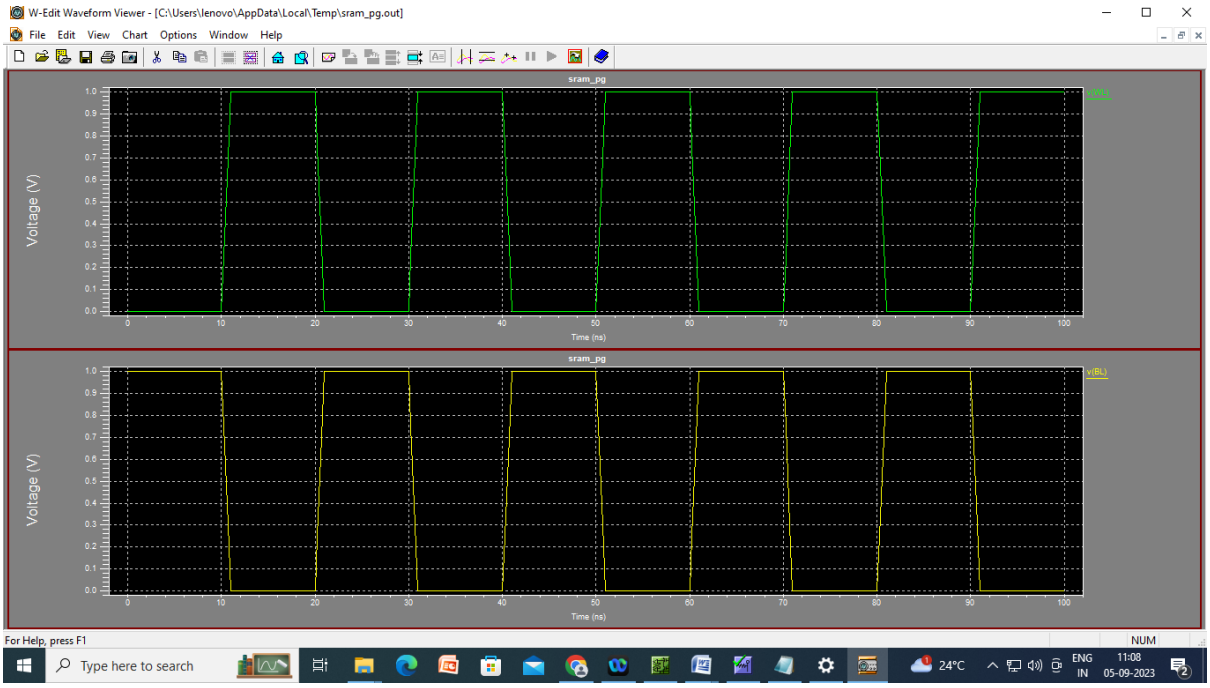


Fig 13: Simulation of PG-SRAM

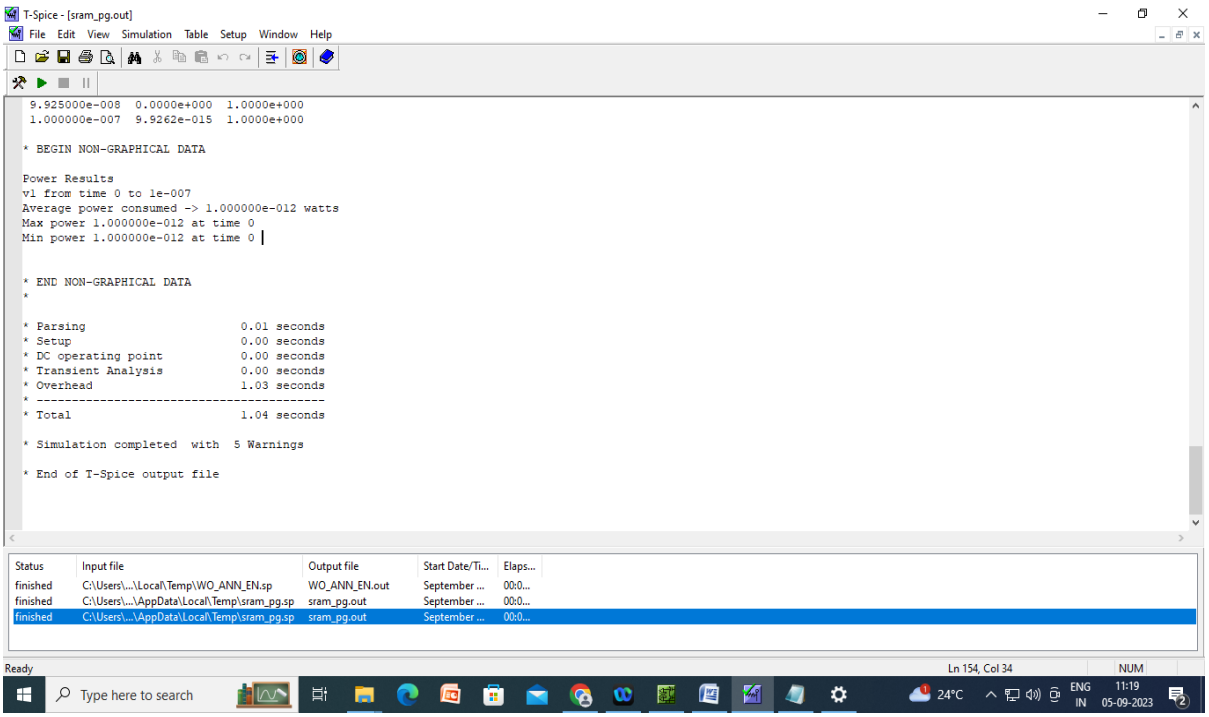


Fig 14: Power results of PG-SRAM

The power dissipation obtained is 1 pw with PG of SRAM circuit. There is a variation of 30 % in power dissipation.

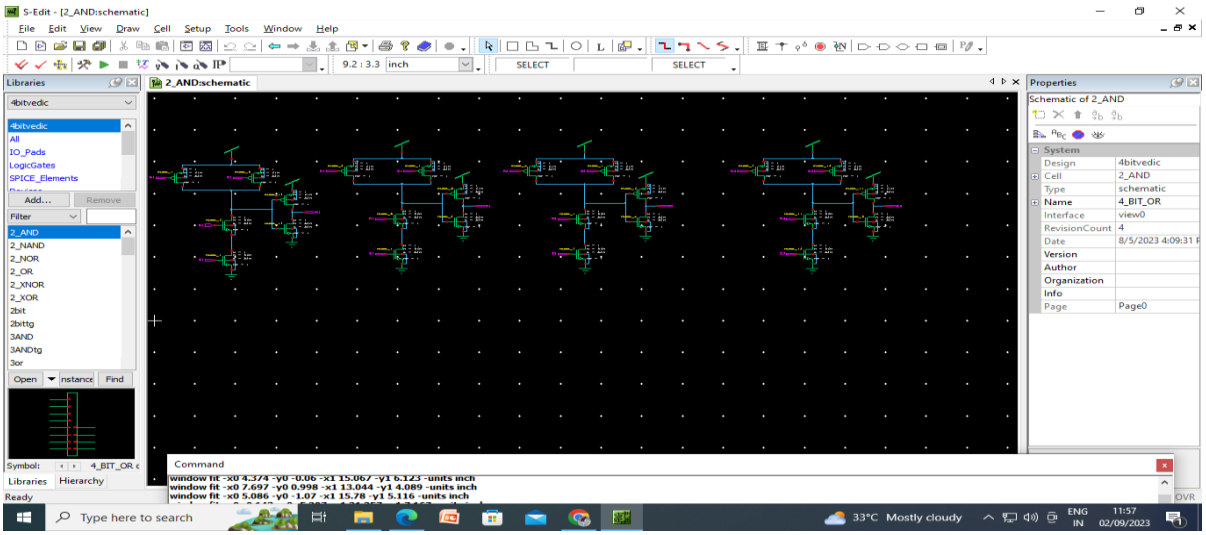


Fig 15: Schematic of 4-bit basic AND

The basic cmos 4-bit AND-gate is revealed in fig 15.

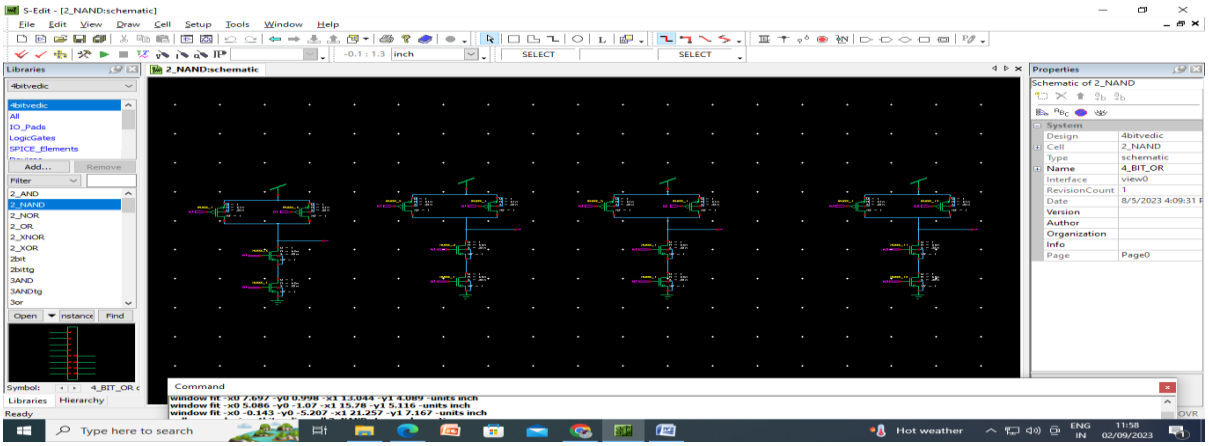


Figure 16: schematic of basic NAND

The necessary cmos 4-bit NAND-gate is illustrated in fig 16.

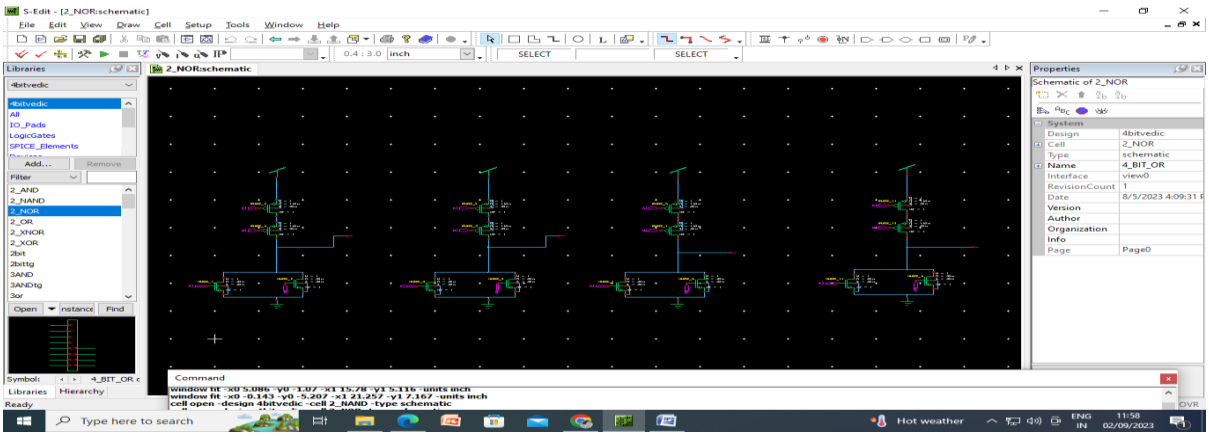


Figure 17: Schematic of basic NOR

The fundamental cmos 4-bit NOR-gate is described in fig 17.

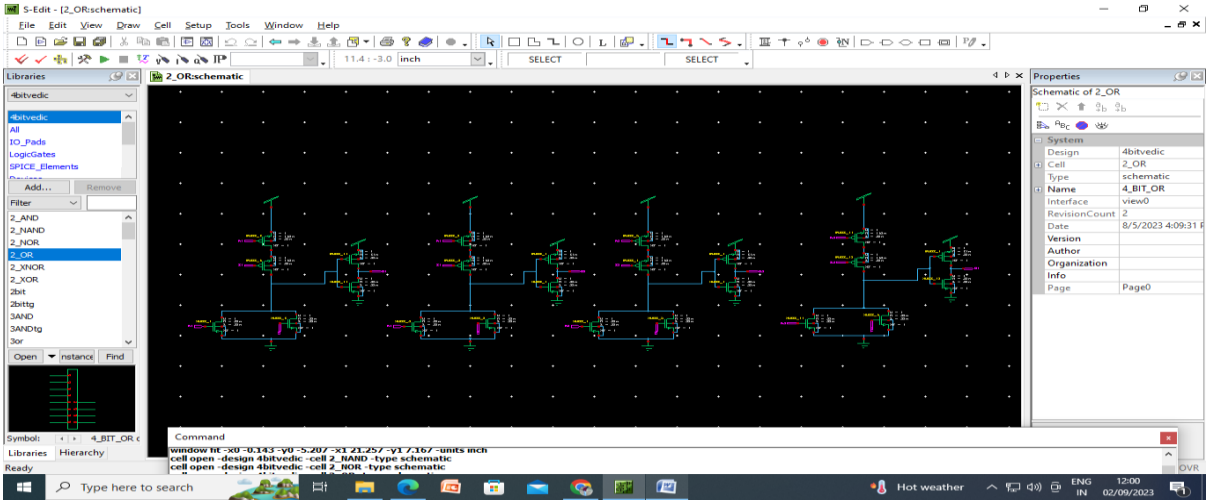


Figure 18: Schematic of basic 4-bit-OR

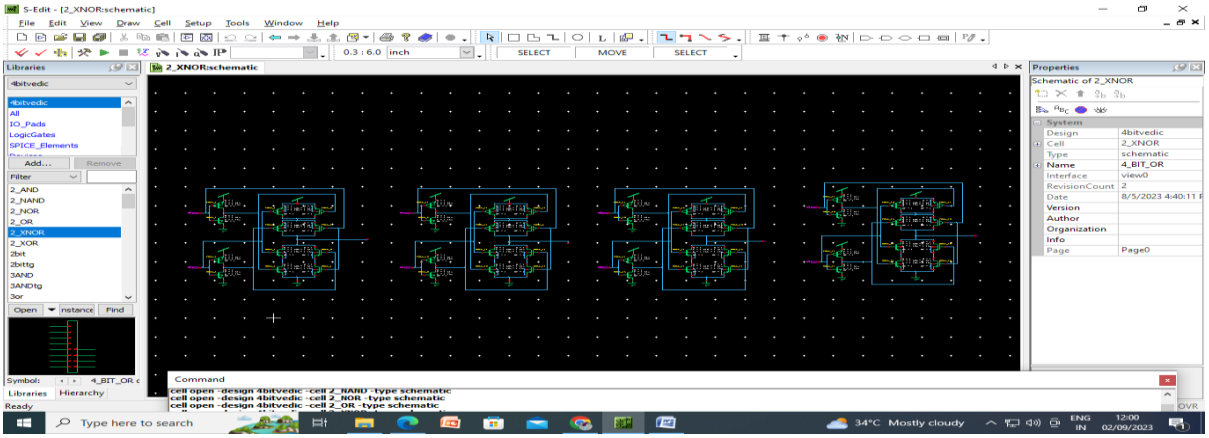


Figure 19: basic 4-bit-Xnor

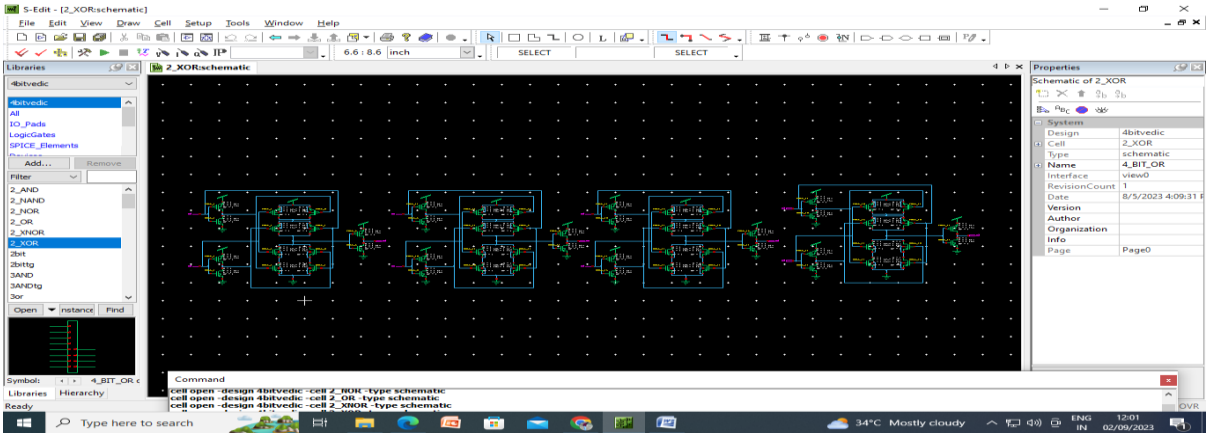


Figure 20: basic 4-bit-XOR

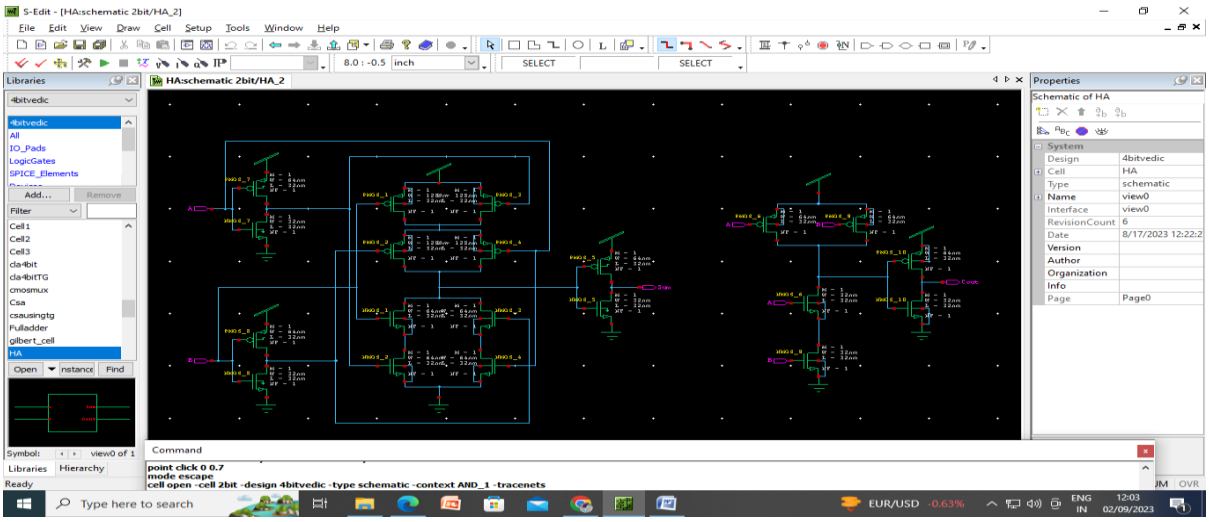


Figure 21: Fundamental half adder schematic

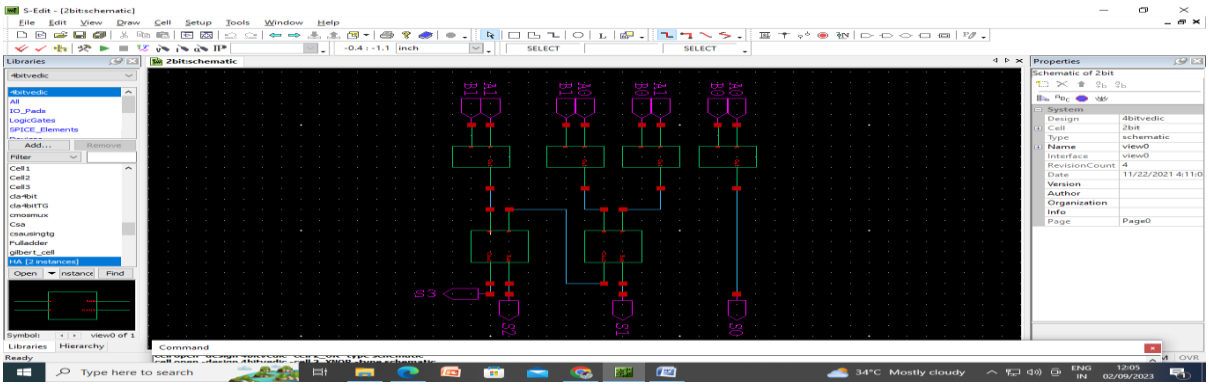


Figure 22: 4-bit half adder

Figure 22 indicates the implemented 4-bit half adder.

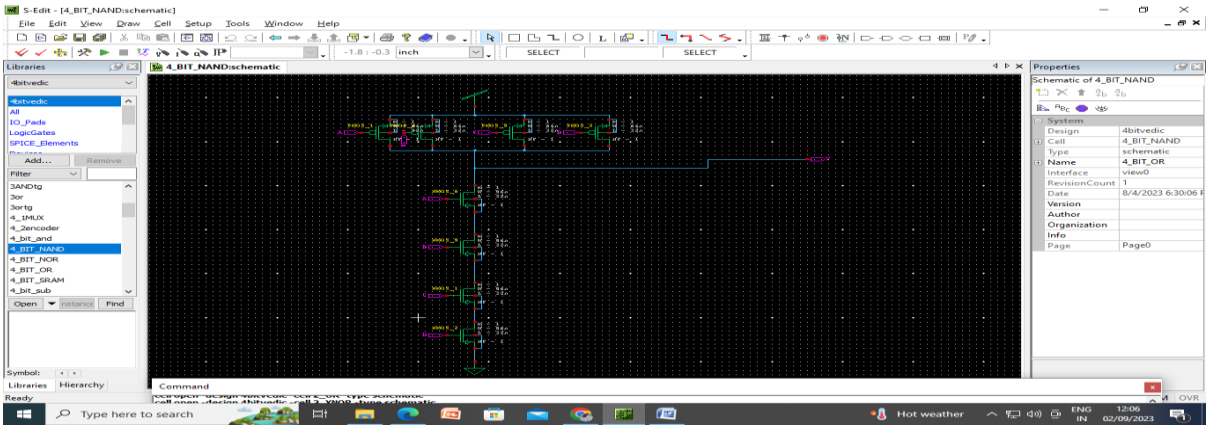


Figure 23:4-bit NAND.

Figure 23 represents the optimized 4-bit NAND.

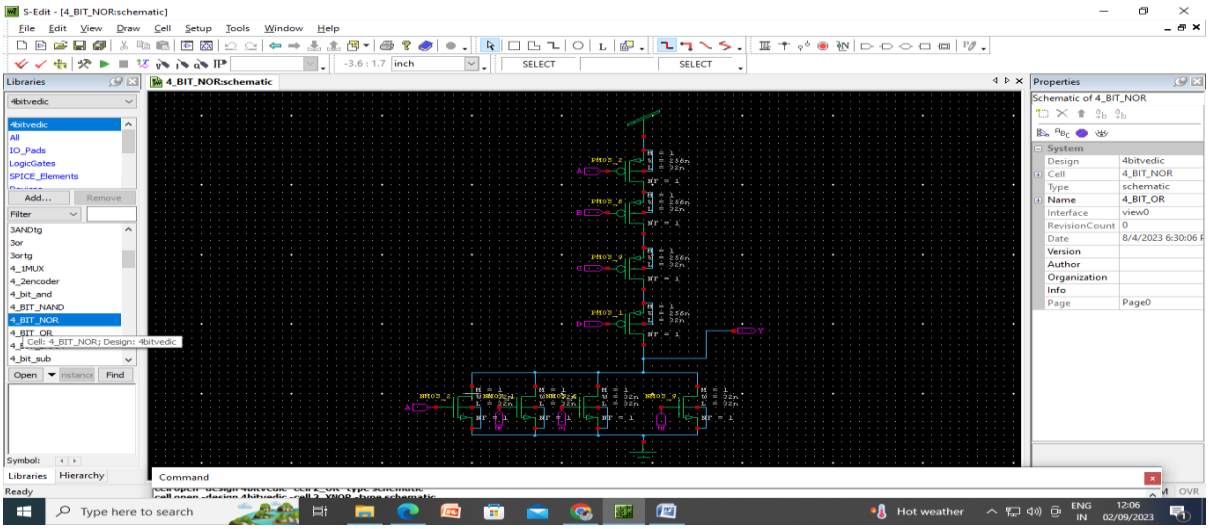


Figure 24:4-bit NOR.

Figure 23 represents the optimized 4-bit NOR.

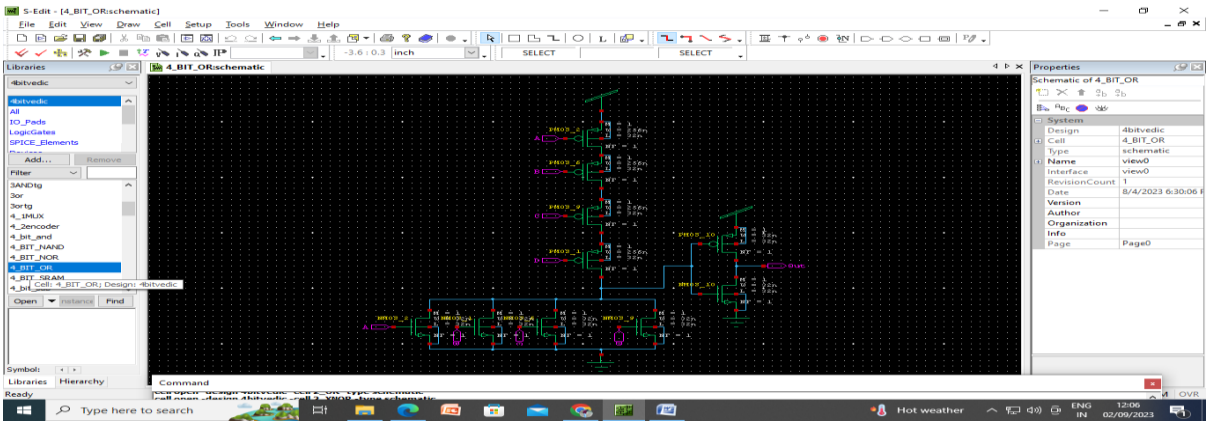


Figure 25:4-bit OR.

Figure 25 represents the optimized 4-bit NOR.

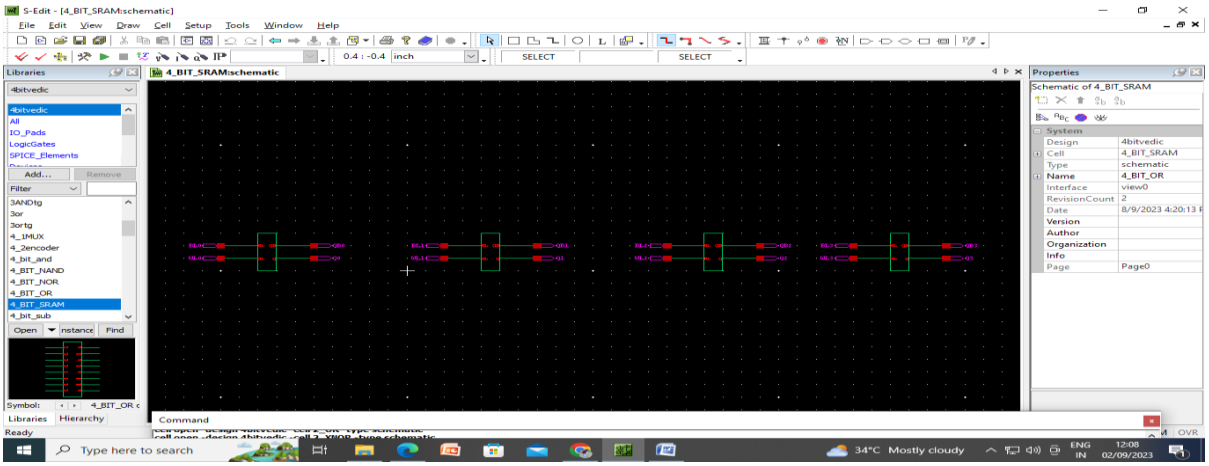


Figure 26: 4-Bit SRAM

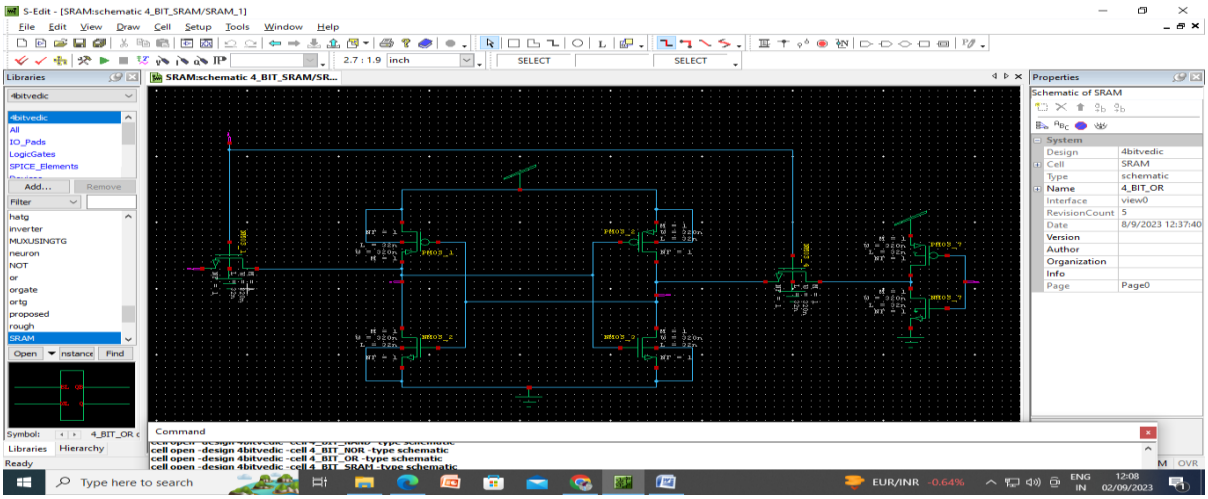
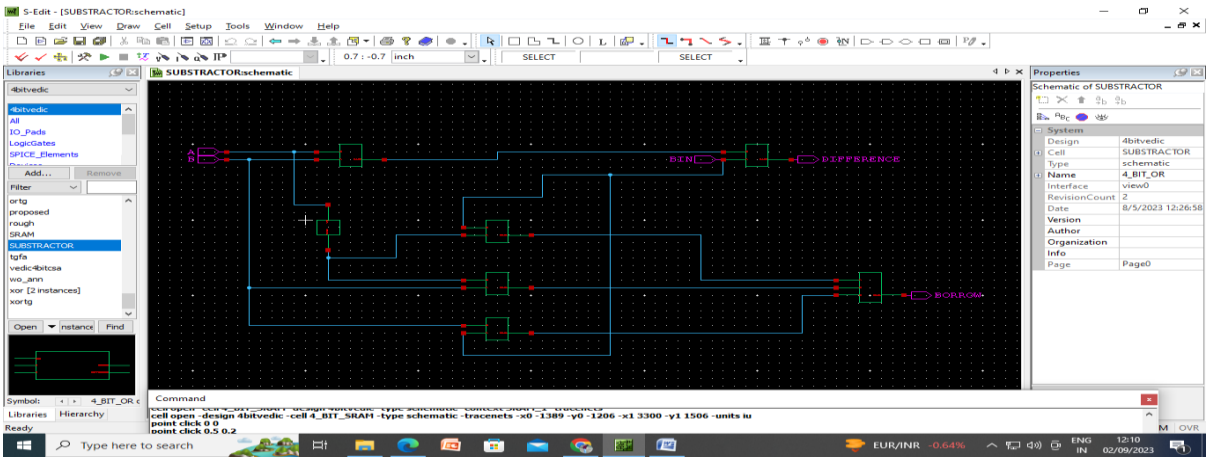


Figure 27: Schematic of fundamental SRAM CELL.



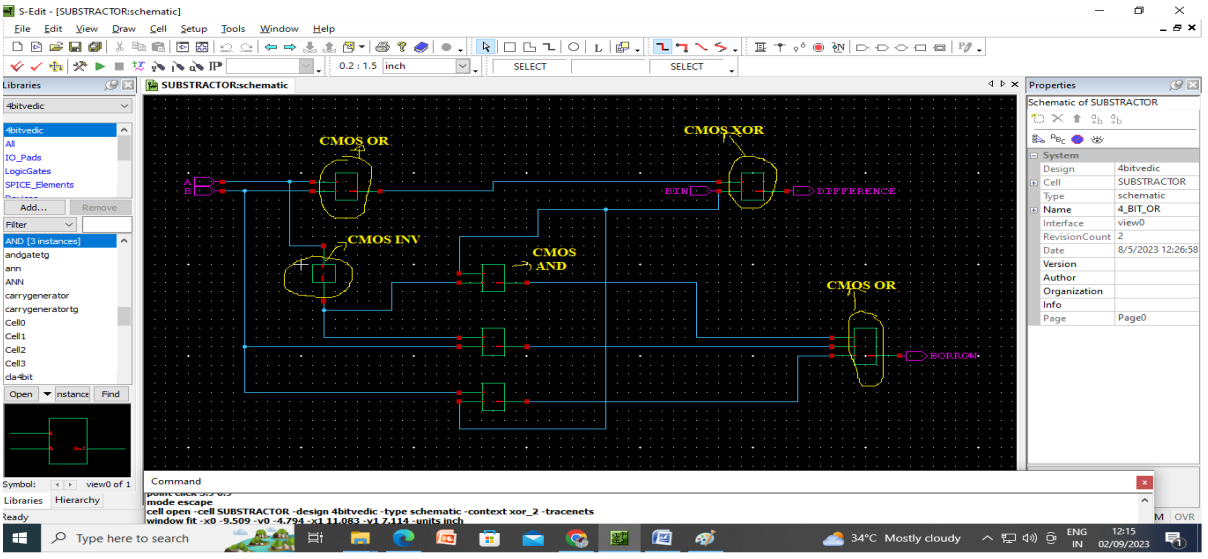


Figure 28: Subtractor

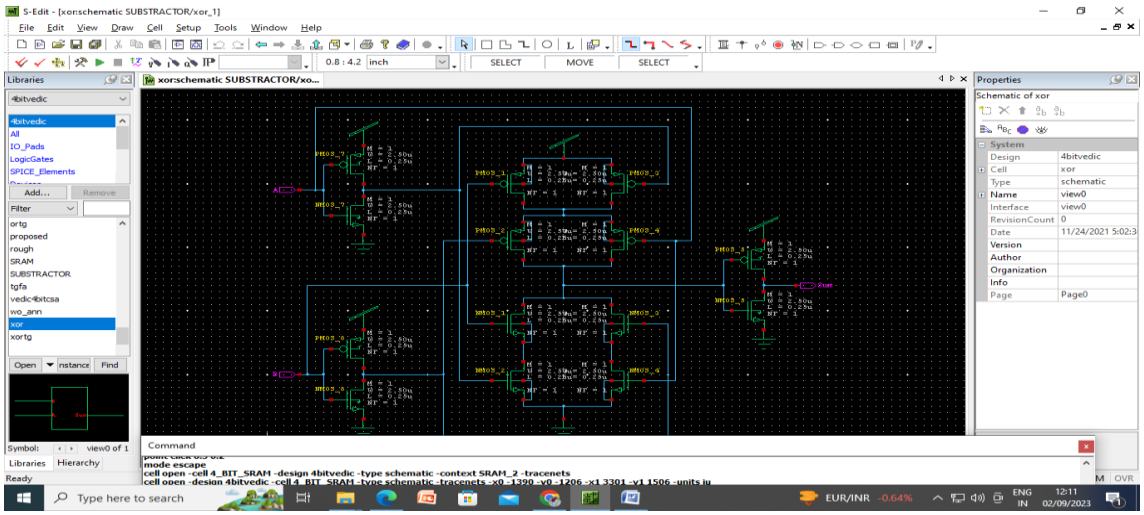


Figure 29: basic block of CMOS OR in subtractor.

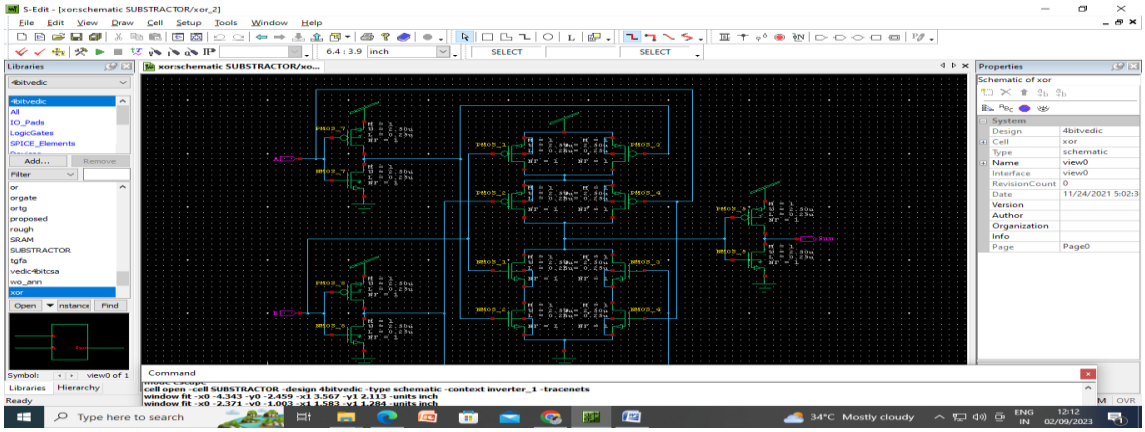


Figure 30: basic block of CMOS CMOS XOR in subtractor.

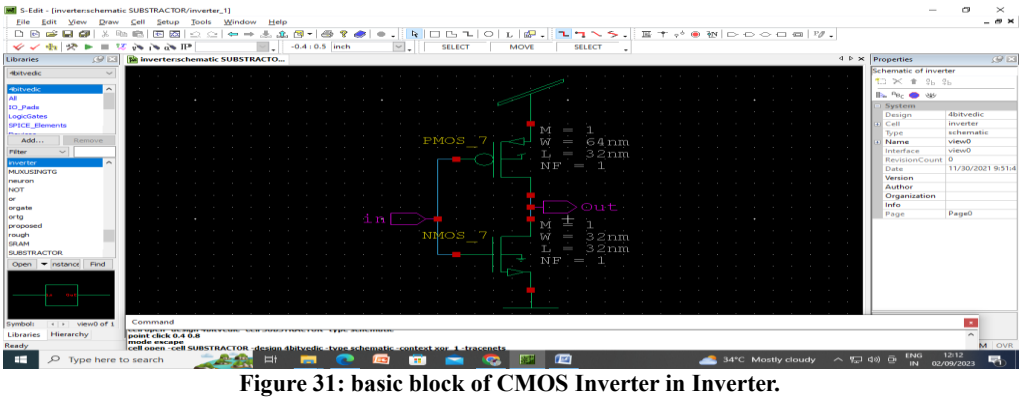


Figure 31: basic block of CMOS Inverter in Inverter.

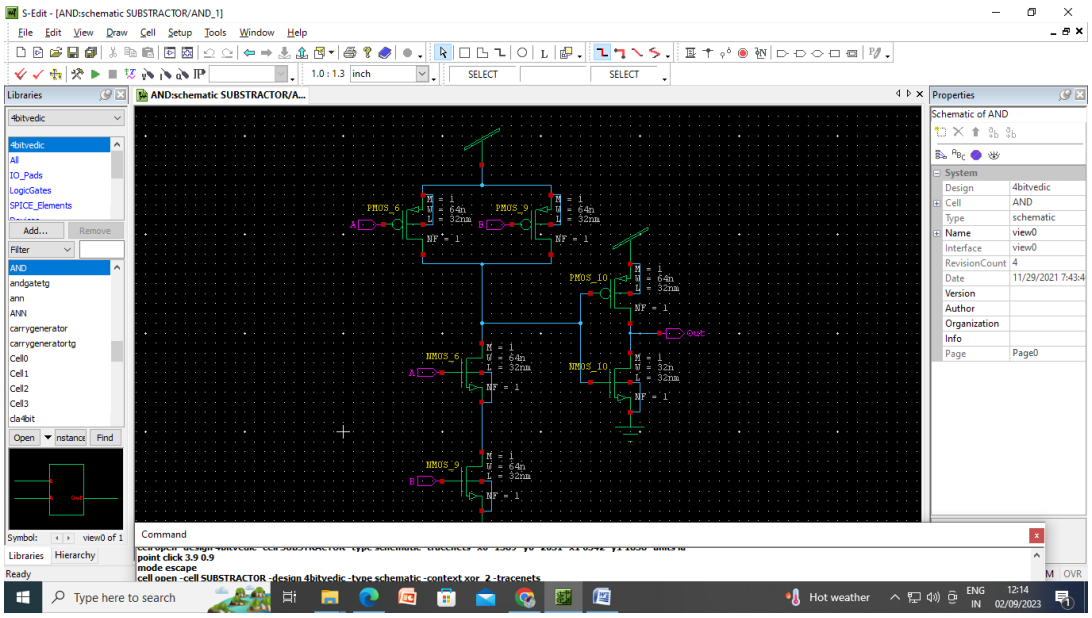


Figure 32: basic block of CMOS AND in Subtractor.

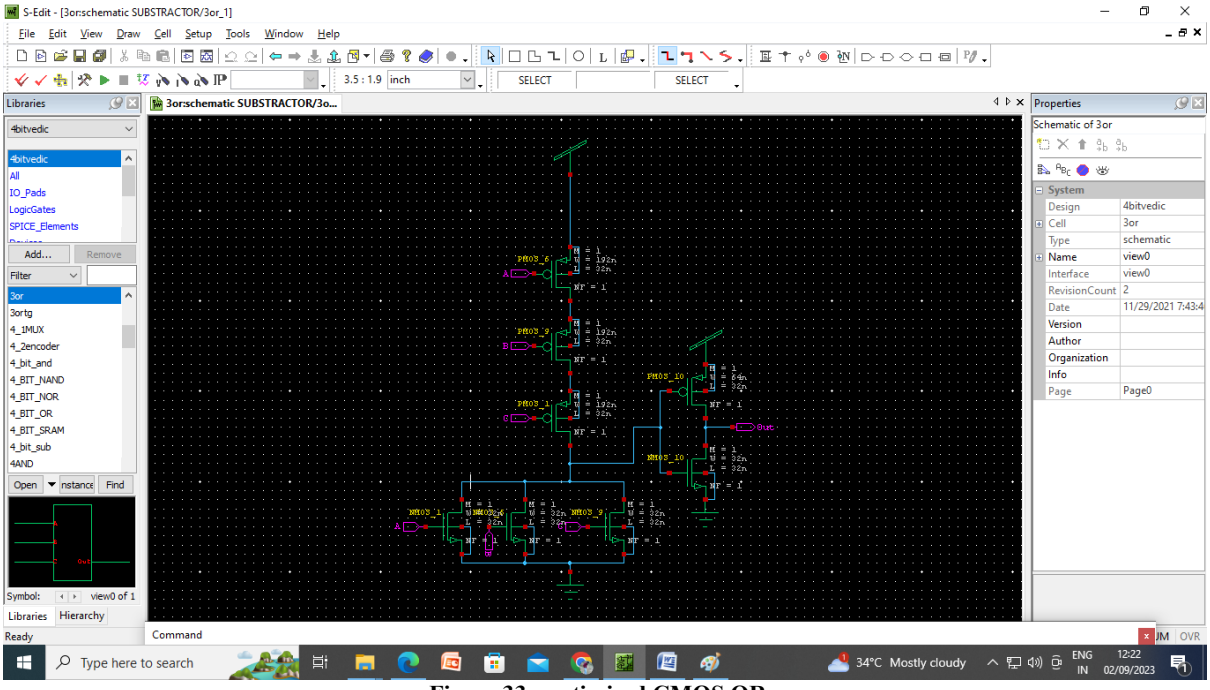


Figure 33: optimised CMOS OR.

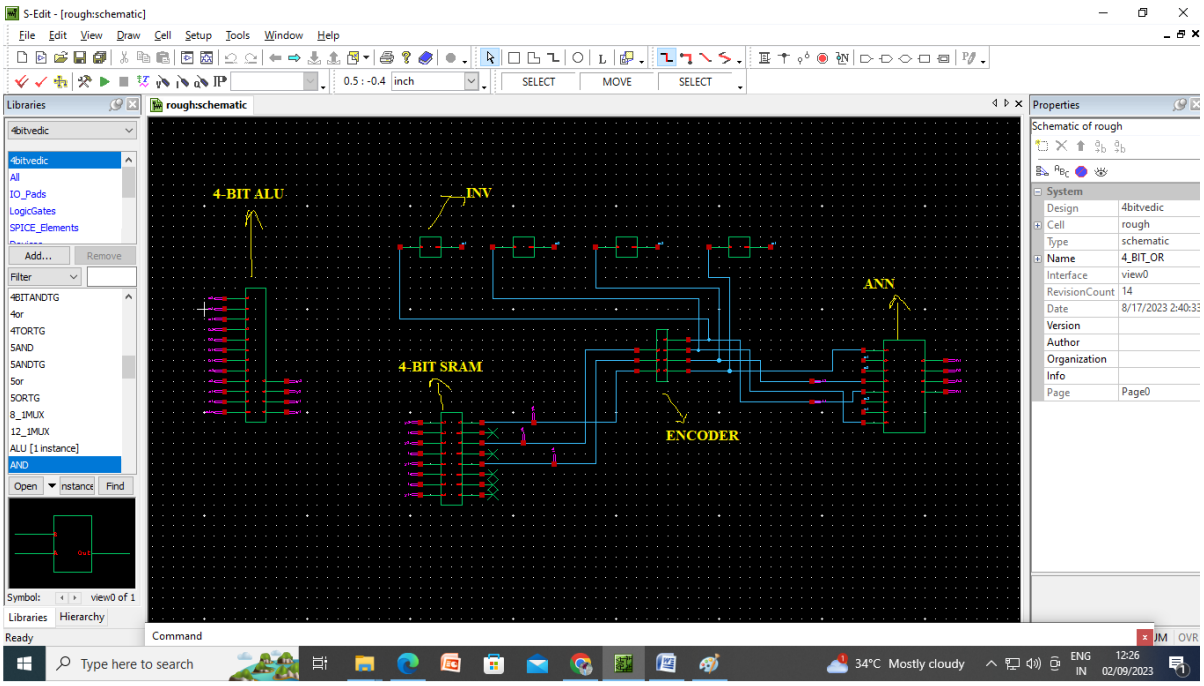


Figure 34: Basic 4-bit processor with ANN.

The sub-blocks are presented in figures 35, 36,37,38,39.

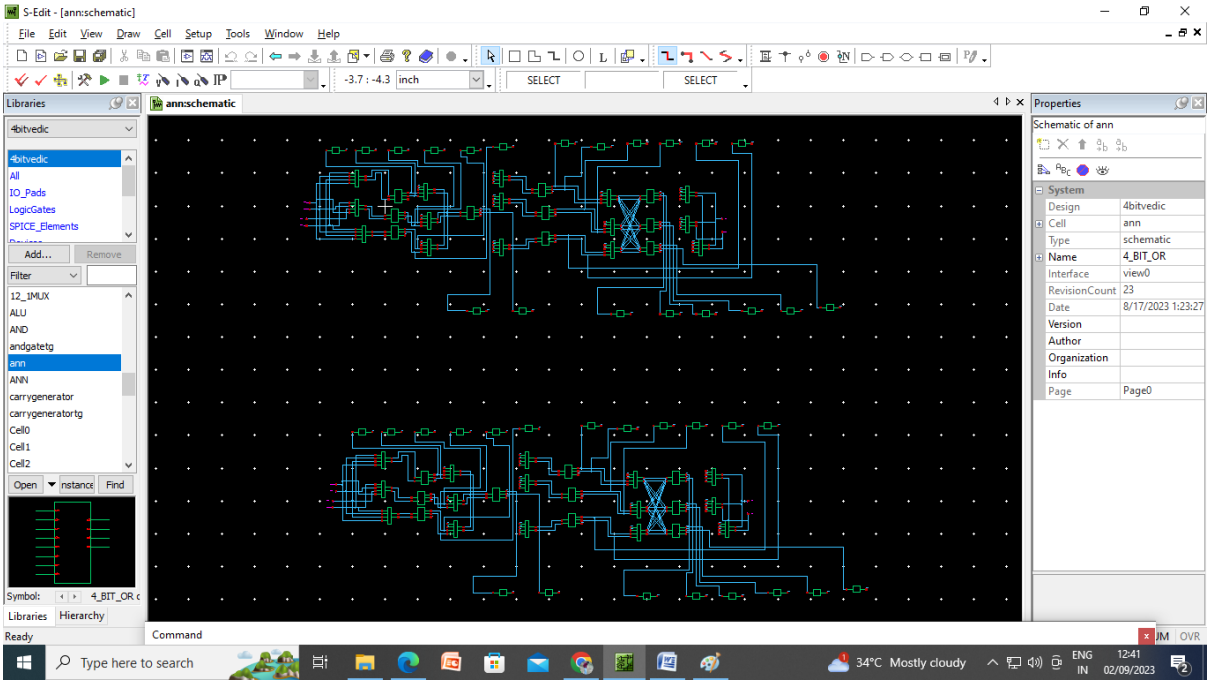


Figure 35: Basic structure of ANN using CMOS.

The above design depicted in fig 35 shows the ANN with basic CMOS blocks

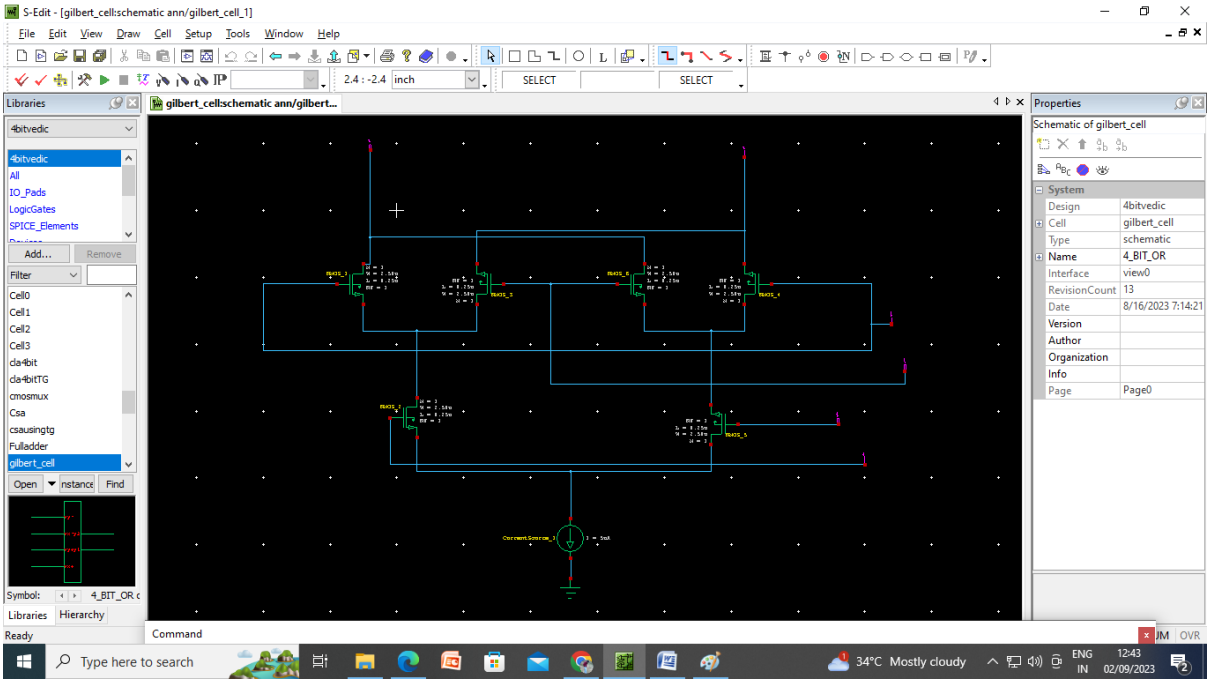


Figure 36: Gilbert CELL

As the multiplier block, the Gilbert cell is employed in the ANN circuitry. Four-quadrant multiplication is possible with the Gilbert multiplier cell, which is an alteration of the emitter coupled cell. As a result, it serves as the foundation for the majority of IC multipliers.

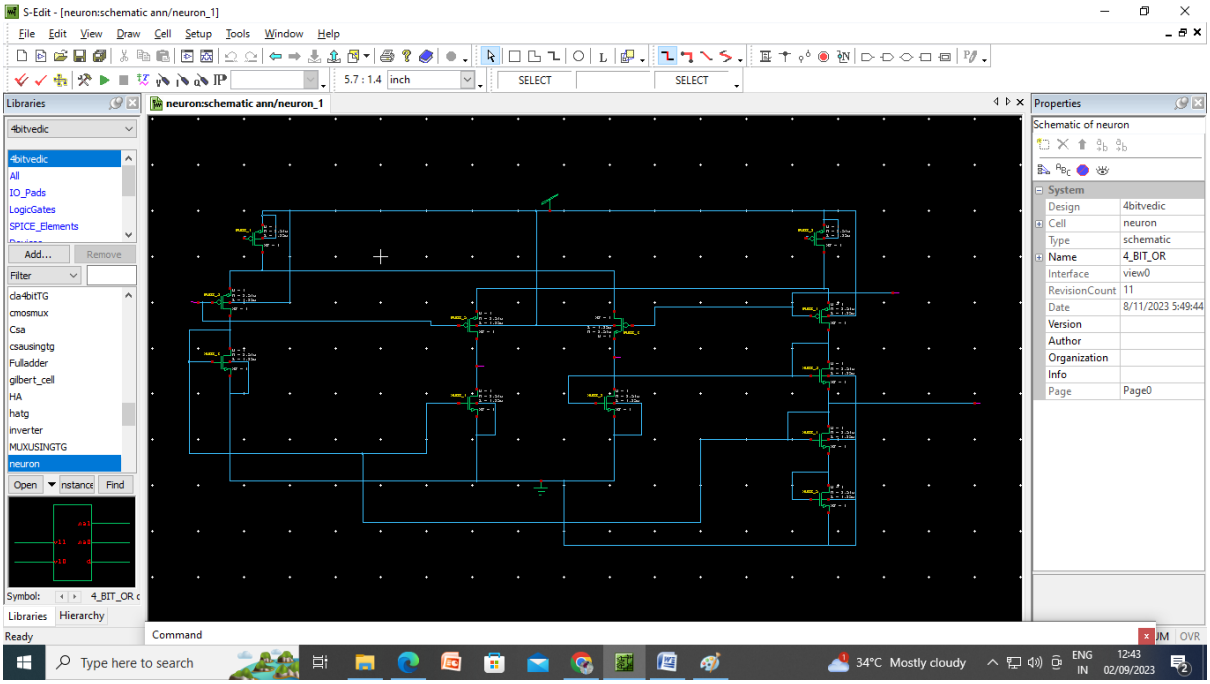


Figure 37: Basic Neuron Cell

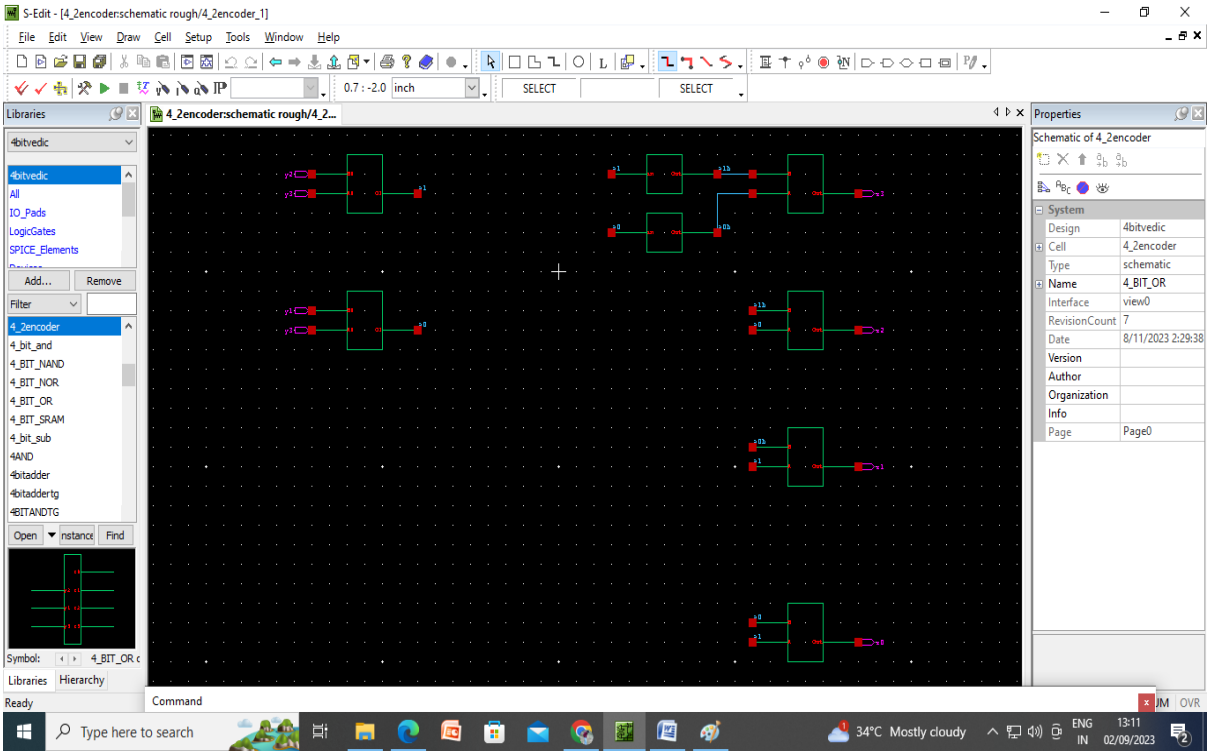


Figure 38: ENCODER

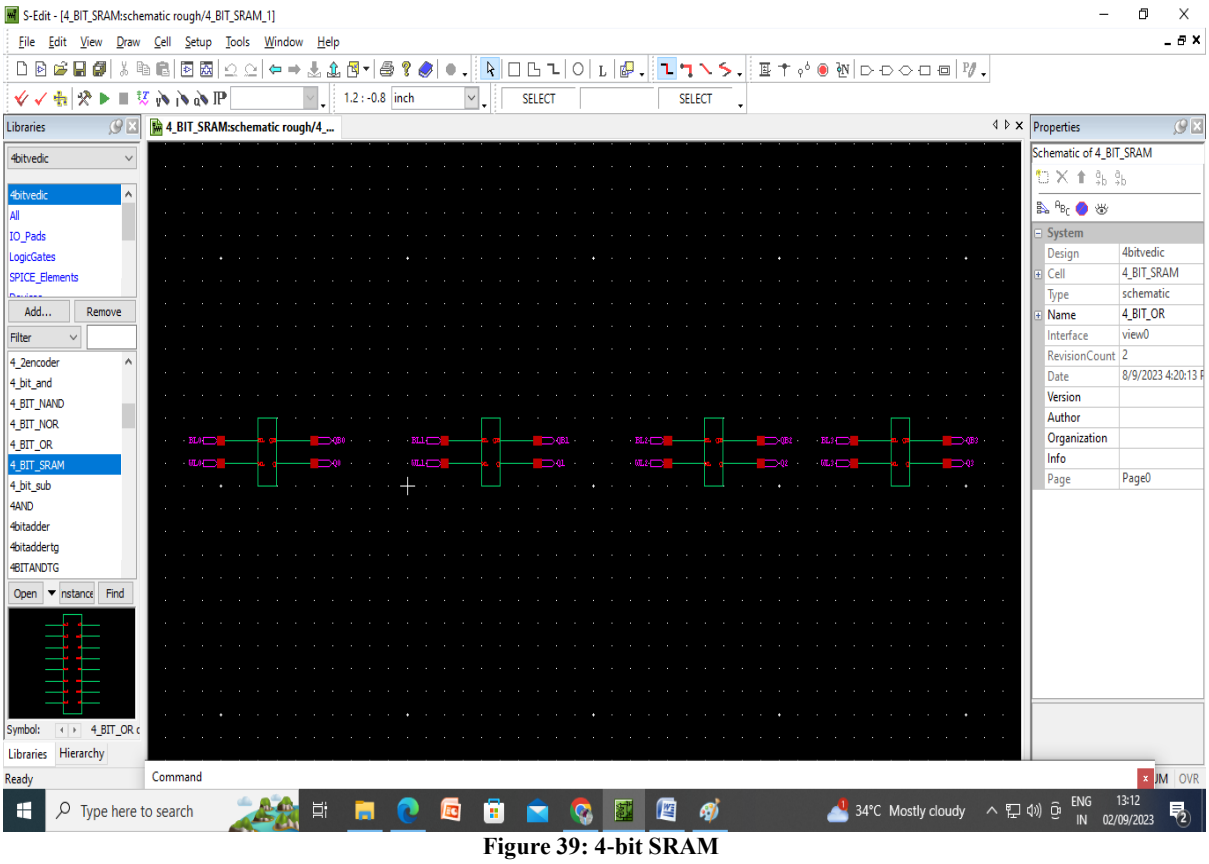


Figure 39: 4-bit SRAM

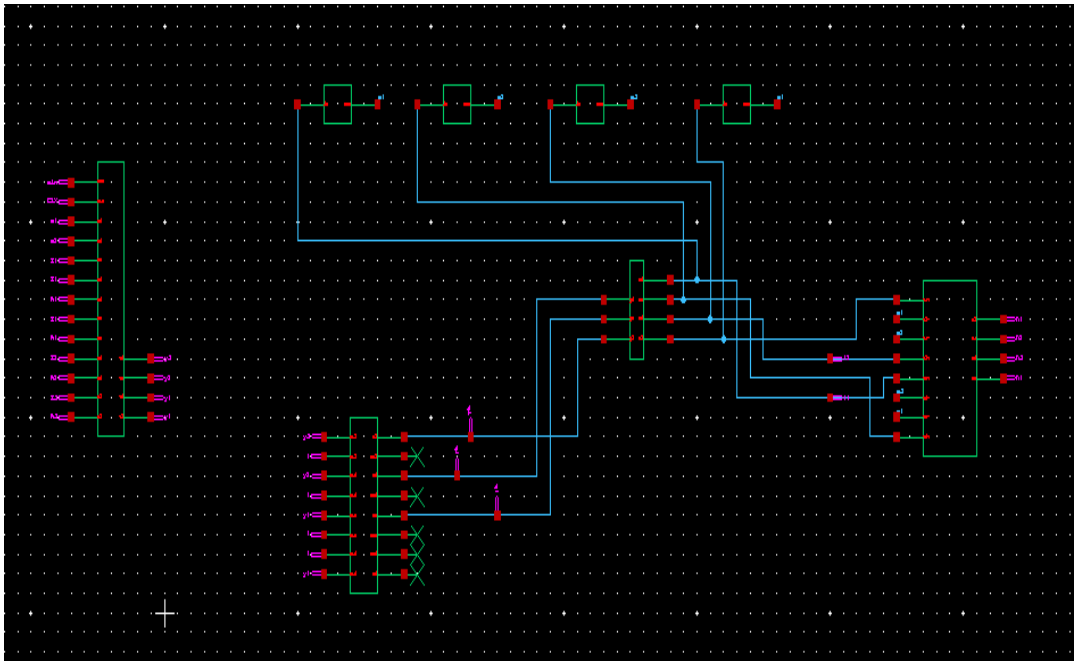


Figure 40: With Clock Gating

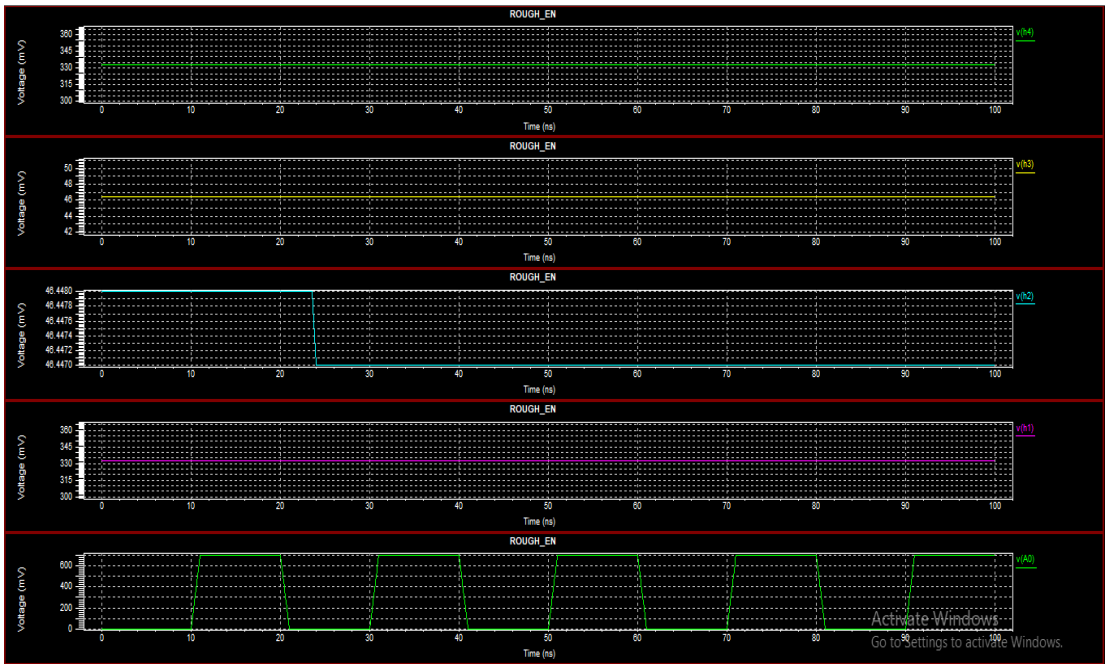


Figure 41: Simulation waveform with Clock Gating

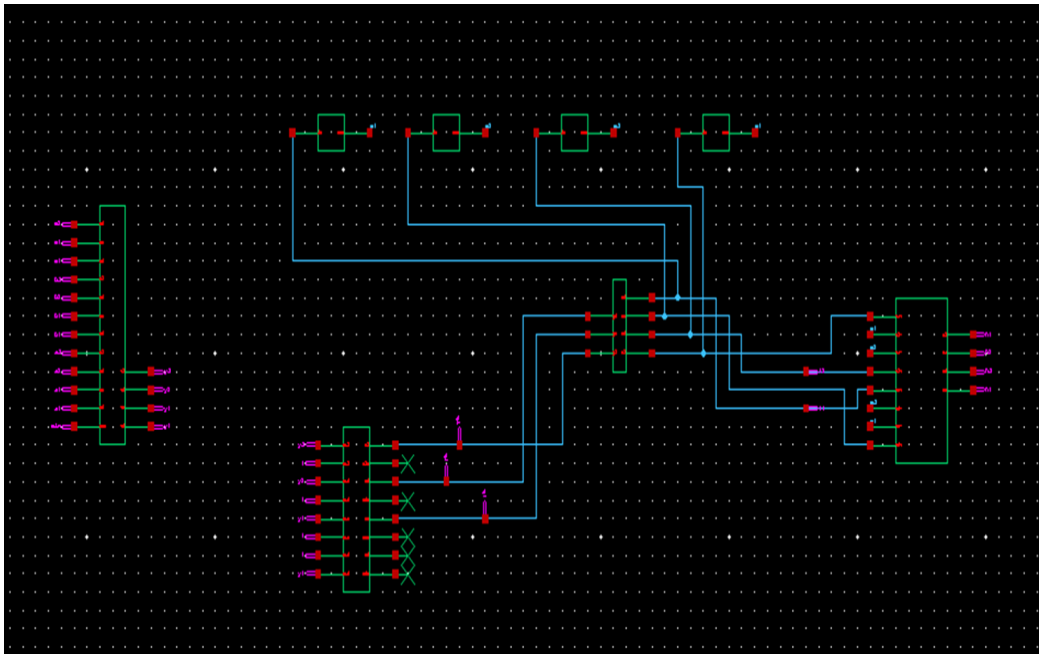


Figure 42: With Power Gating

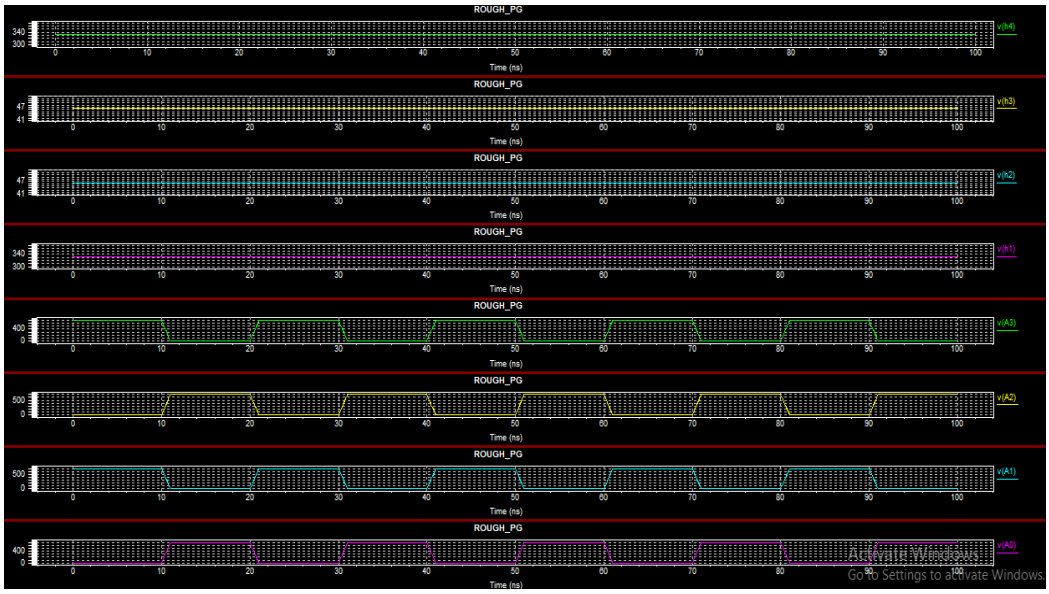


Figure 43: Simulation waveform with Power Gating

```
* BEGIN NON-GRAPHICAL DATA

Power Results
v1 from time 0 to 1e-007
Average power consumed -> 5.211081e-003 watts
Max power 6.205597e-003 at time 4.07875e-008
Min power 4.930157e-003 at time 1.16345e-008


* END NON-GRAPHICAL DATA


* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

delay = not found
  Trigger = 1.0571e-008
  Target  = not found

* END NON-GRAPHICAL DATA
```

Figure 44: Power Results with 45nm

```
* BEGIN NON-GRAPHICAL DATA

Power Results
v1 from time 0 to 1e-007
Average power consumed -> 2.788101e-004 watts
Max power 6.719861e-004 at time 7.08596e-008
Min power 1.081531e-004 at time 6.025e-008


* END NON-GRAPHICAL DATA


* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

delay = 6.8672e-011
  Trigger = 1.0571e-008
```

Figure 45: Power values with 32nm

CONCLUSION:

Below tables represents the comparison of area and power values of the proposed design.

SL.NO	TECHNIQUE	NO OF MOSETS	POWER
1	**WITHOUT ANN**	880	2.788101e-004W
2	**WITHOUT ANN_CG**	1048	4.489172e-006W
3	**WITHOUT ANN_PG**	1048	2.155765e-004W

SL.NO	TECHNIQUE	NO OF MOSETS	POWER
1	**WITH ANN**	1380	6.044845e-004W
2	**WITH ANN_CG**	1548	6.044895e-006W
3	**WITH ANN_PG**	1548	5.344917e-004W

With the above results we can conclude that for the proposed result with and without CG,PG, ANN we got prominent results when compared with existing approaches[1,2,3,4,13,15]. The circuit blocks of design are represented. Clock gating is a power optimization technique commonly used in digital circuit design, including Arithmetic Logic Units . The primary goal of clock gating is to reduce power consumption by selectively disabling the clock signal to certain circuit elements when they are not actively needed. Clock gating can be applied to specific parts of the unit to minimize power consumption during idle or low-activity periods, based on the current operation requirements. The clock gating logic operates dynamically based on the ALU's current state and the specific operation being executed. When the ALU is idle or waiting for a new operation, clock gating can be applied to reduce power consumption during these periods. By selectively disabling the clock to parts of the ALU when they are not needed, power consumption is reduced. CG introduces additional complexity to the design. Power gating involves inserting switches into the power supply lines of specific circuit blocks. When a particular block is not actively needed, the power switch is turned off, disconnecting the power supply and isolating the block from the rest of the circuit. In the work[15] the power dissipationed was 0.1541nw, in [13] it is 5.9414mw

REFERENCES:

1. Sujata. A.A, Lalitha. Y.S, “Design and performance analysis of 4-bit Nano-Processor design for low area, low power and minimum delay using 32nm FinFET technology”, WSEAS TRANSACTIONS on ELECTRONICS, DOI: 10.37394/232017.2021.12.1
2. K. Prasad Babu, Dr. K.E. Sreenivasa Murthy, Dr. M.N. Giri Prasad, “Design of CMOS Digital-Processor using Hybrid Technique”, 10.1109/ICACCS51430.2021.9441689, IEEEXPLORE.
3. K. Prasad Babu, Dr. K.E. Sreenivasa Murthy, Dr. M.N. Giri Prasad, “Design of CMOS Digital-Processor Using Clock Gating”, vol1,2022, TELEMATIQUE Pg.No.2488 – 2510, ISSN: 1856-4194

4. K. Prasad Babu, Dr. K.E. Sreenivasa Murthy, Dr. M.N. Giri Prasad, “Implementation of Power Gated Alu For Low Power Processor”, Journal BIOGECKO (ISSN: 2230-5807), Vol 12 Issue 01 2023, Pg.No: 765-780.
5. DALIA EL-DIB,et.at, "Procedures of Low Power Digital Design: A Survey", Wseas
6. Transactions On Electronics, E-ISSN: 2415-1513, Volume 9, 2018.
7. Aqilah binti Abdul Tahrim,et.al, "Plan and Performance Analysis of 1-Bit FinFET Full Adder Cells for Subthreshold Region at 16 nm Process Technology", Hindawi Publishing Corporation Journal of Nanomaterials,Volume 2015, Article ID 726175. 13 pages, http://dx.doi.org/10.1155/2015/726175.
8. Debajit Bhattacharya,at.al, "FinFETs: From Devices to Architectures", Hindawi Publishing Corporation, Advances in Electronics, Volume 2014, Article ID 365689, 21 pages, http://dx.doi.org/10.1155/2014/365689.
9. G.Saranya, R.S. Kiruthika Optimized Design Of An Alu Block Using Architectural Level Of Power Optimization Techniques 3/1/2011 IEEE XPLORE 168-172.
10. Jinhui Wang, Na Gong Pns-Fcr:Flexible Charge Recycling Dynamic Circuit Technique For Low Power Microprocessors 2/1/2016 Ieee Transactions On Vlsi Vol 24 No.2 613-624.
11. A J Ryan Philips “4-Bit Microprocessor: Design, Simulation, Fabrication, and Testing”Volume 18, Issue 1 (2009) Microelectronic Engineering Conference 2009, pages 81-91.
12. Suchismita Sengupta, Partha Sarkar, Ananya Dastidar, “Design of a 4 Bit Arithmetic & Logic Unit, Evaluation of Its Performance Metrics & its Implementation in a Processor”,
13. 978-1-7281-6221-8/20/$31.00 ©2020 IEEE, Pg.No: 1-8.
14. Wenheng Ma , Qiao Cheng, Yudi Gao, Lan Xu and Ningmei Yu, “An Ultra-Low-Power Embedded Processor with Variable Micro-Architecture”, Micromachines 2021, 12, 292. https://doi.org/10.3390/mi12030292. P.g. No: 1-16.
15. Vegha. B N, Dr. Vijay Prakash, “Design and Implementation of 4-Bit ALU for Low-Power using Adiabatic Logic based on FINFET”,International Journal of Engineering Research & Technology (IJERT),ISSN: 2278-0181,Vol. 9 Issue 07, July-2020,Pg.No: 649-656.
16. JunHa Suk, ChanYeop Ahn, S M Mojahidul Ahsan and SoYoung Kim, “A stable 4-bit ALU design for printed devices”, Flexible and Printed Electronics,Vol7,Number 1, DOI 10.1088/2058-8585/ac49da,ISSN: 2058-8585,
17. Mary Sajin Sanju.I, M. Vadivel, “Performance Evaluation of an Efficient ALU”, Nanotechnology Perceptions 19 No.2 (2023) 10–18, ISSN 1660-6795.
18. K.Prasad Babu, Dr. K.E. Sreenivasa Murthy, Dr. M.N. Giri Prasad, “A Study & Analysis on low Power processor Design Using Various Techniques”, Jornal of propulsion technology,ISSN:1001-4055, vol 44, no 3 2023, pg no :2355-2379.

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